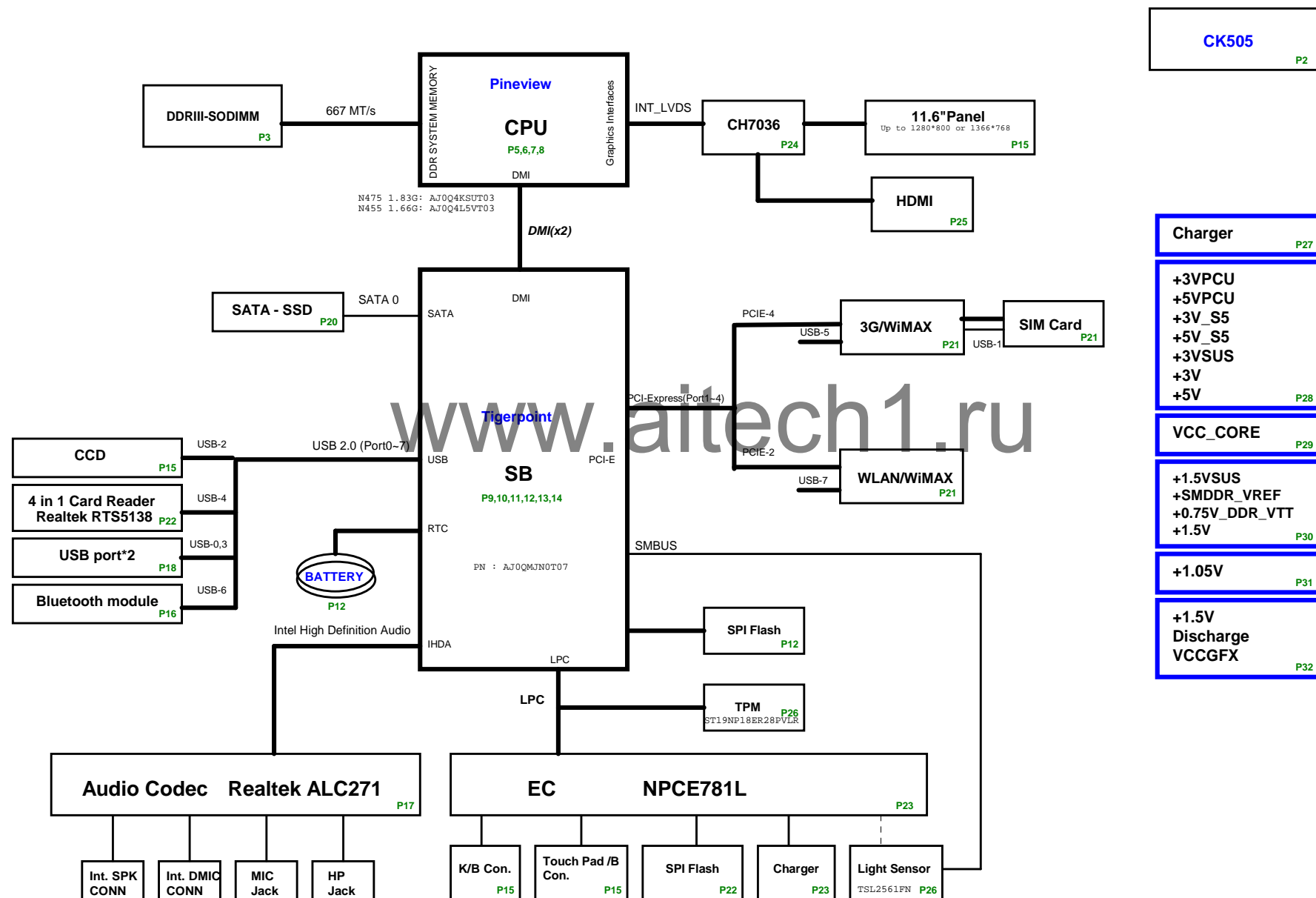
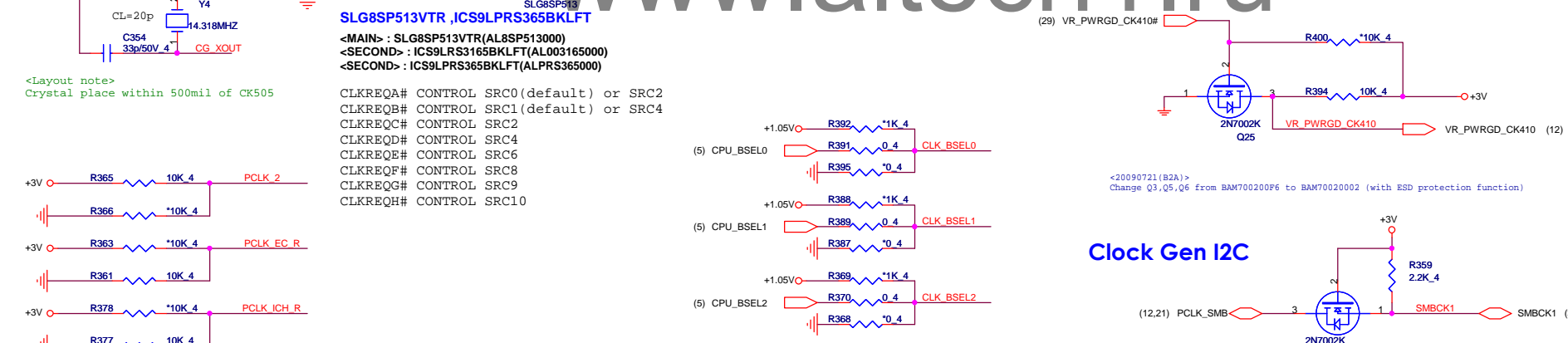
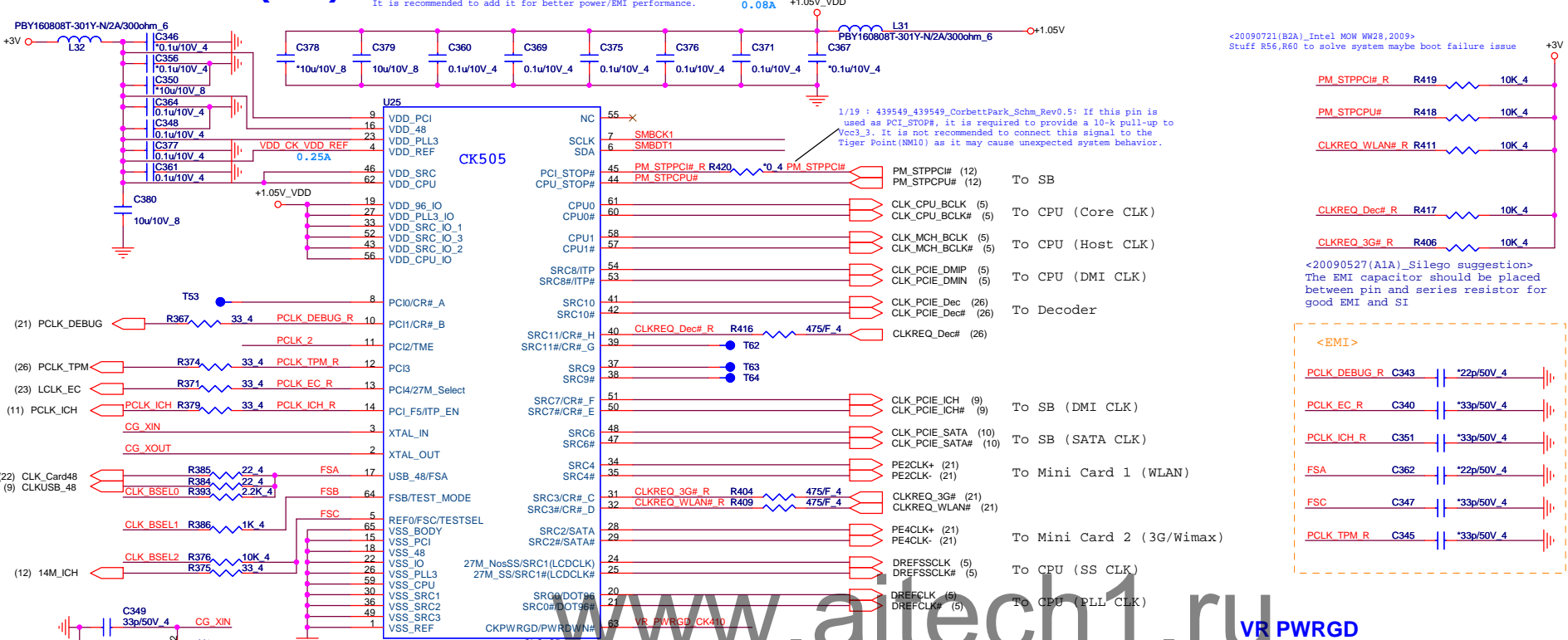


ZGA Block Diagram

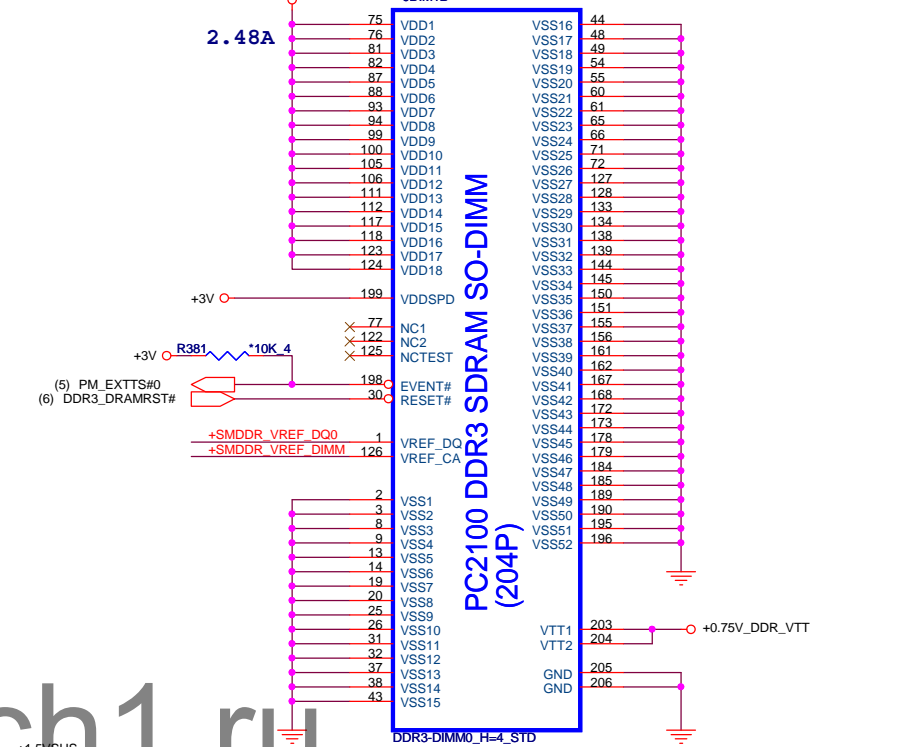
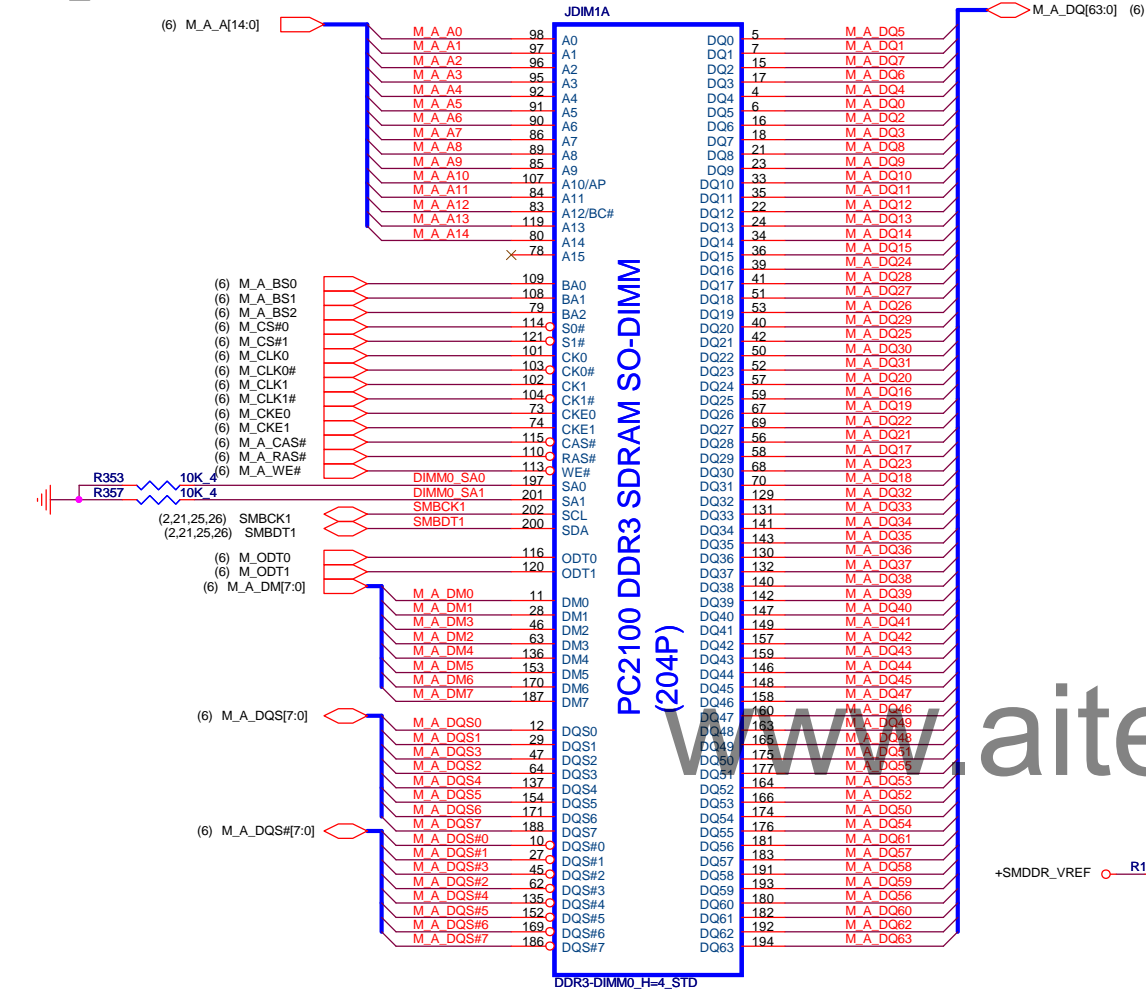


Clock Generator(CLK)

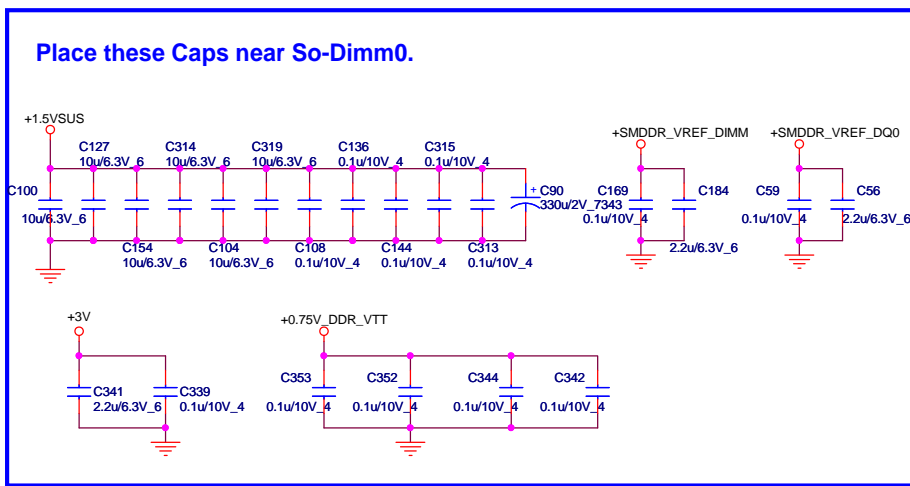
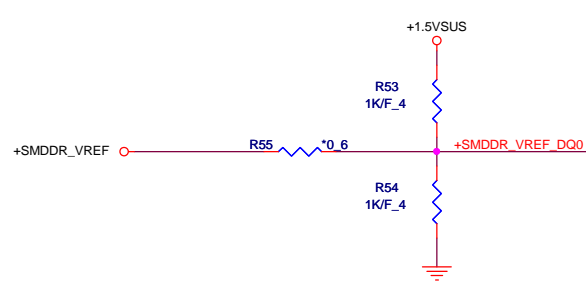
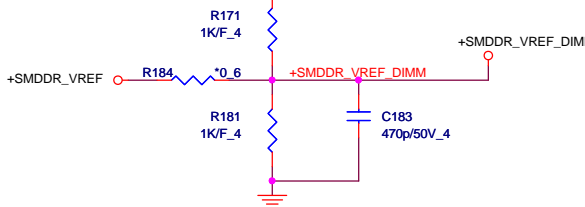


FSC	FSB	FSA	CPU	SRC	PCI	REF	USB	DOT
BSEL2	BSEL1	BSEL0						
0	0	0	266.66	100	33.33	14.318	48	96
0	0	1	133.33	100	33.33	14.318	48	96
0	1	0	200.00	100	33.33	14.318	48	96
0	1	1	166.66	100	33.33	14.318	48	96
1	0	0	333.33	100	33.33	14.318	48	96
1	0	1	100.00	100	33.33	14.318	48	96
1	1	0	400.00	100	33.33	14.318	48	96
1	1	1						
RESERVED								

DDR_STD (DDR)



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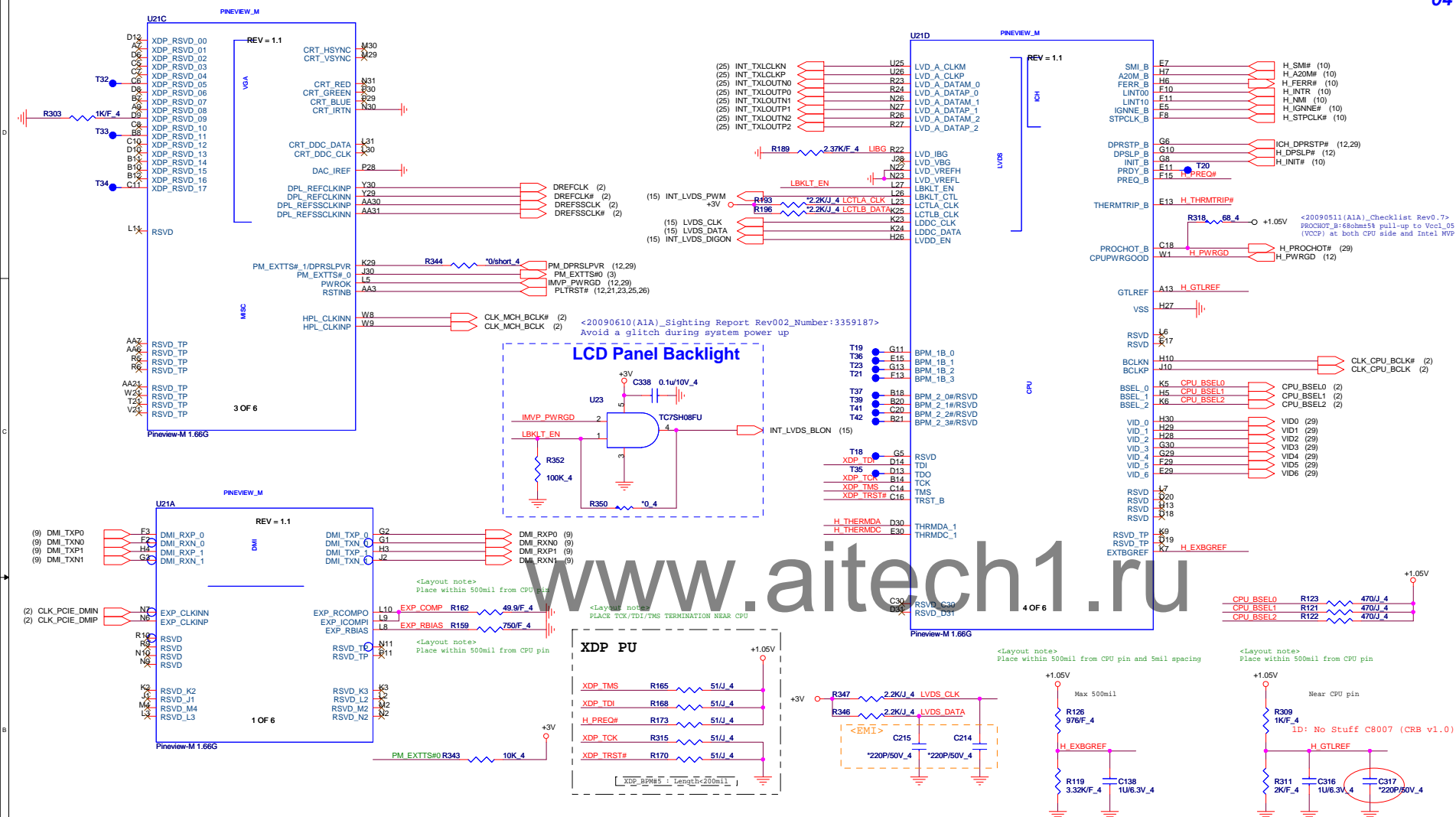
www.aitech1.ru



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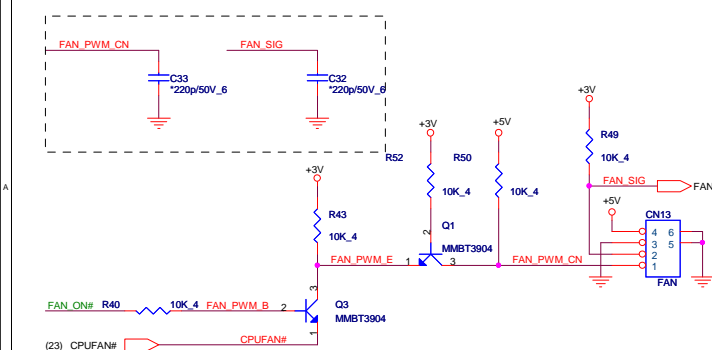
PROJECT : ZGA

Size	Document Number	Rev
	BLANK	1A
Date:	Wednesday, July 07, 2010	Sheet 4 of 38

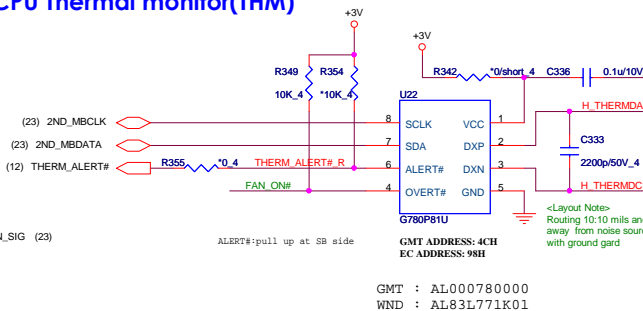


CPU FAN CTRL(THM)

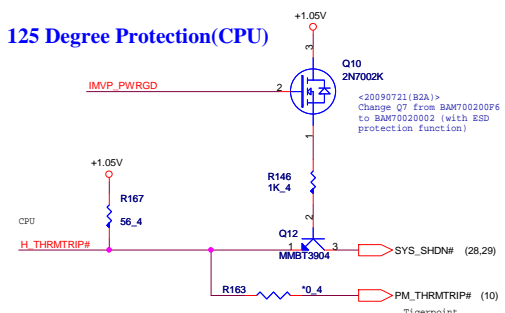
8/11 B-test : for EMI

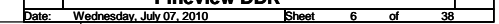


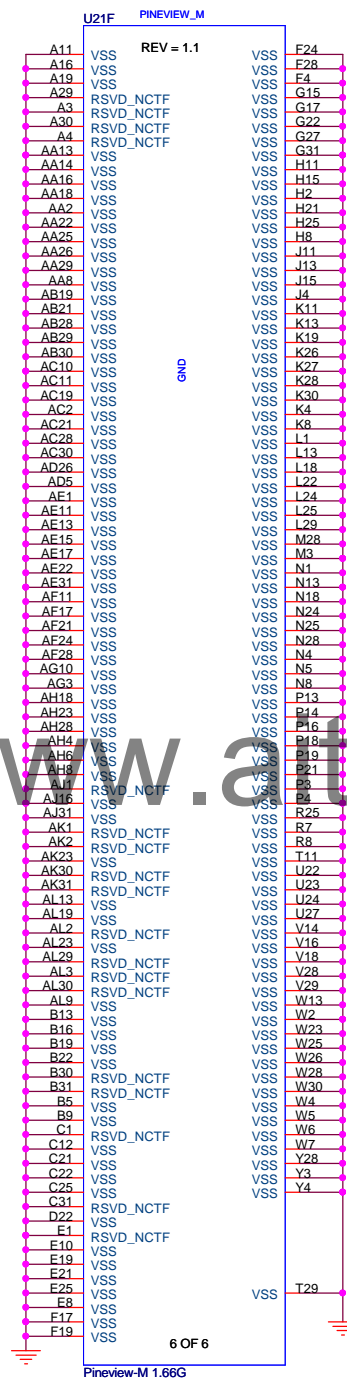
CPU Thermal monitor(THM)



125 Degree Protection(CPU)





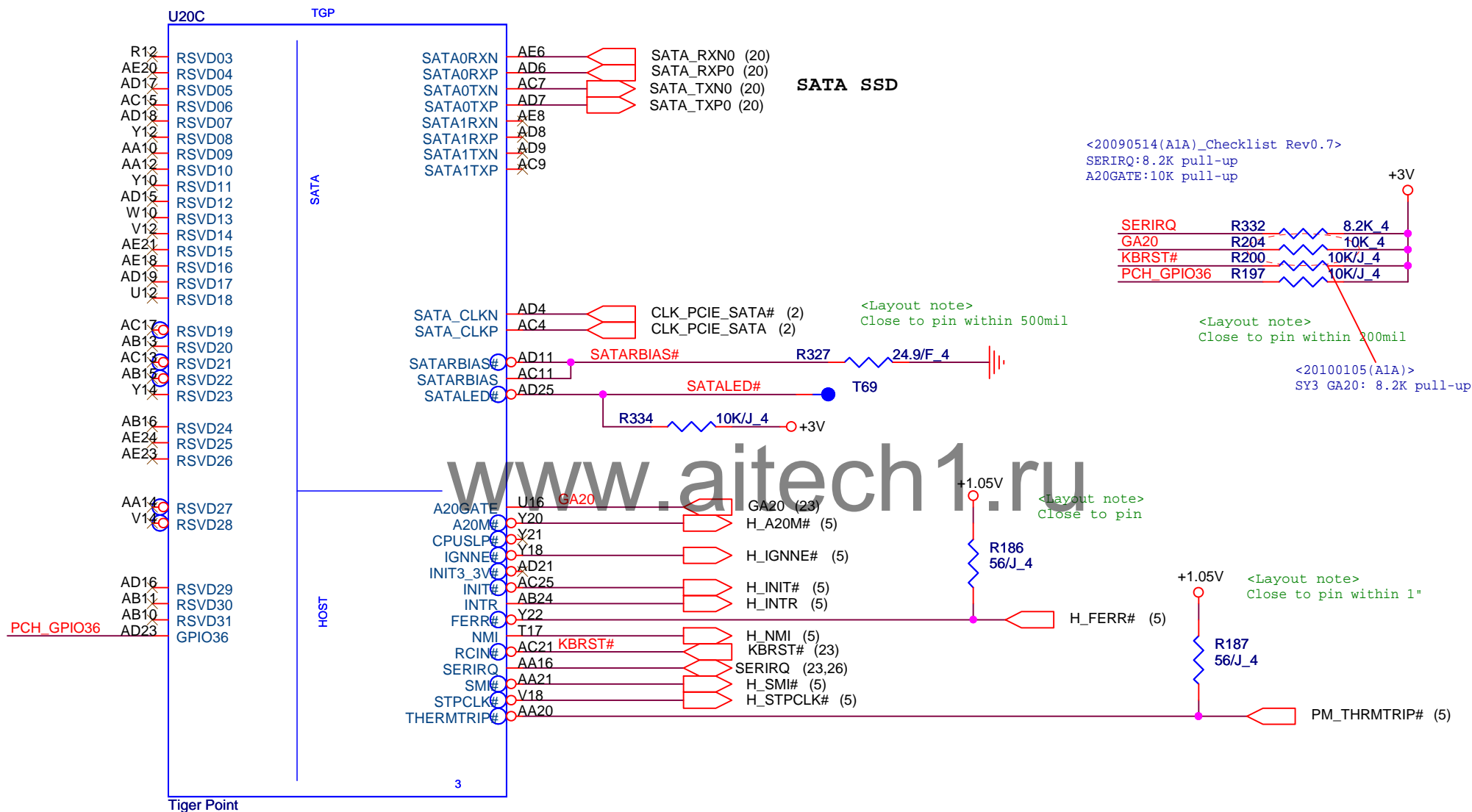


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PROJECT : ZGA

Size	Document Number	Rev 1B
Pineview GND		
Date:	Wednesday, July 07, 2010	Sheet 8 of 38





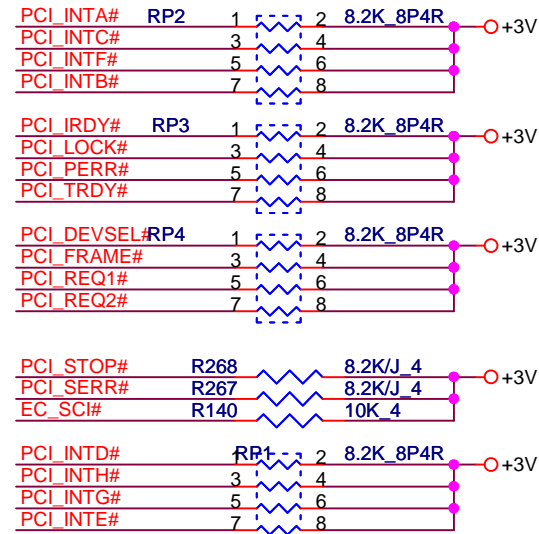
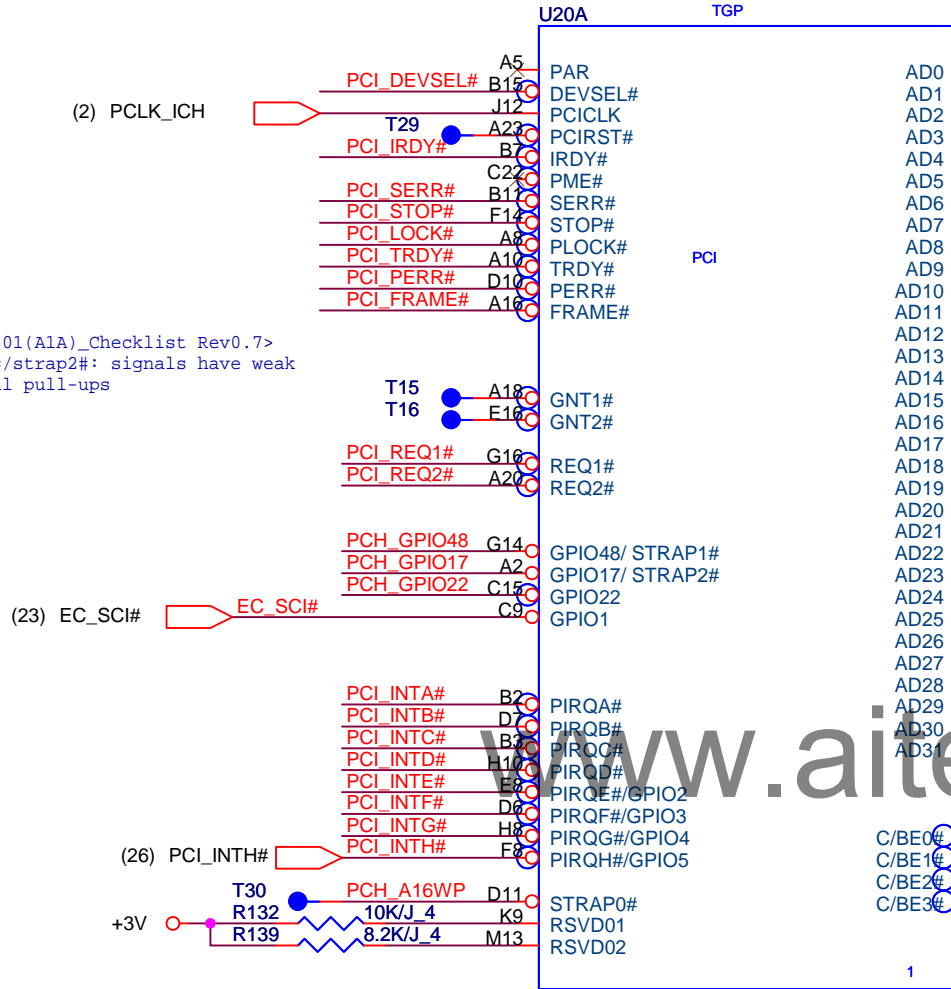
Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
		1B
Date:	Wednesday, July 07, 2010	Sheet 10 of 38

Tiger Point Sata/Host

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak
internal pull-ups



IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI (Default)
1	0	PCI
1	1	LPC



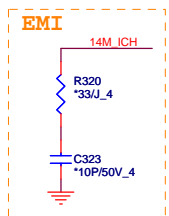
A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
-----------------------	---

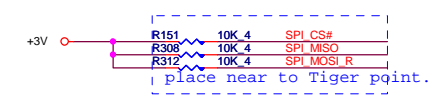
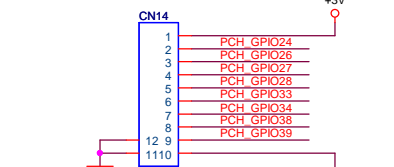
Quanta Computer Inc.

PROJECT : ZGA

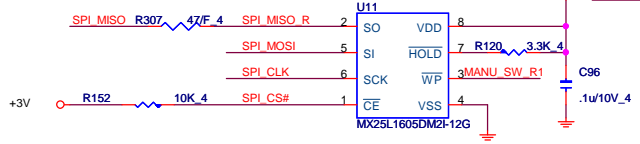
Size	Document Number	Rev 1B
TigerPoint PCI(3/6)		
Date:	Wednesday, July 07, 2010	Sheet 11 of 38



debug port for google require

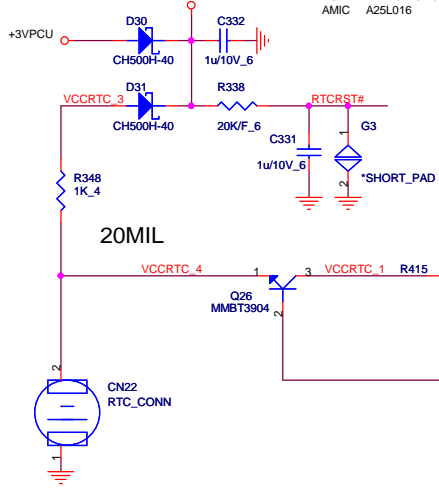


SPI FLASH(CLG)



1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

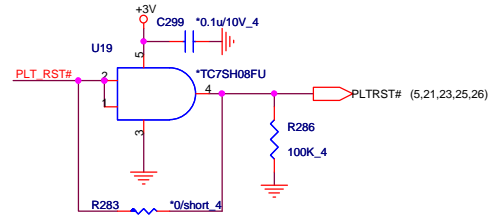
RTC(RTC)



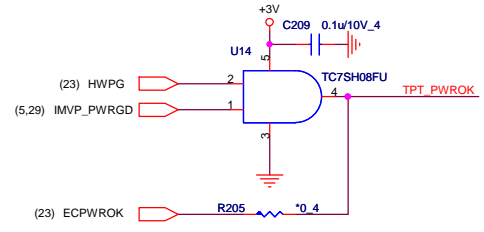
At 11/24 add
Winbond W25X16AVSSIG
MXIC MX25L1605AM2C-15G
EON EN25F16-100HIP
AMIC A25L016

AKE38ZP0N01
AKE37FP0Z13
AKE38ZAD000
AKE38ZN0800

Platform Reset



TPT Power OK



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s (1 port/4 lanes)

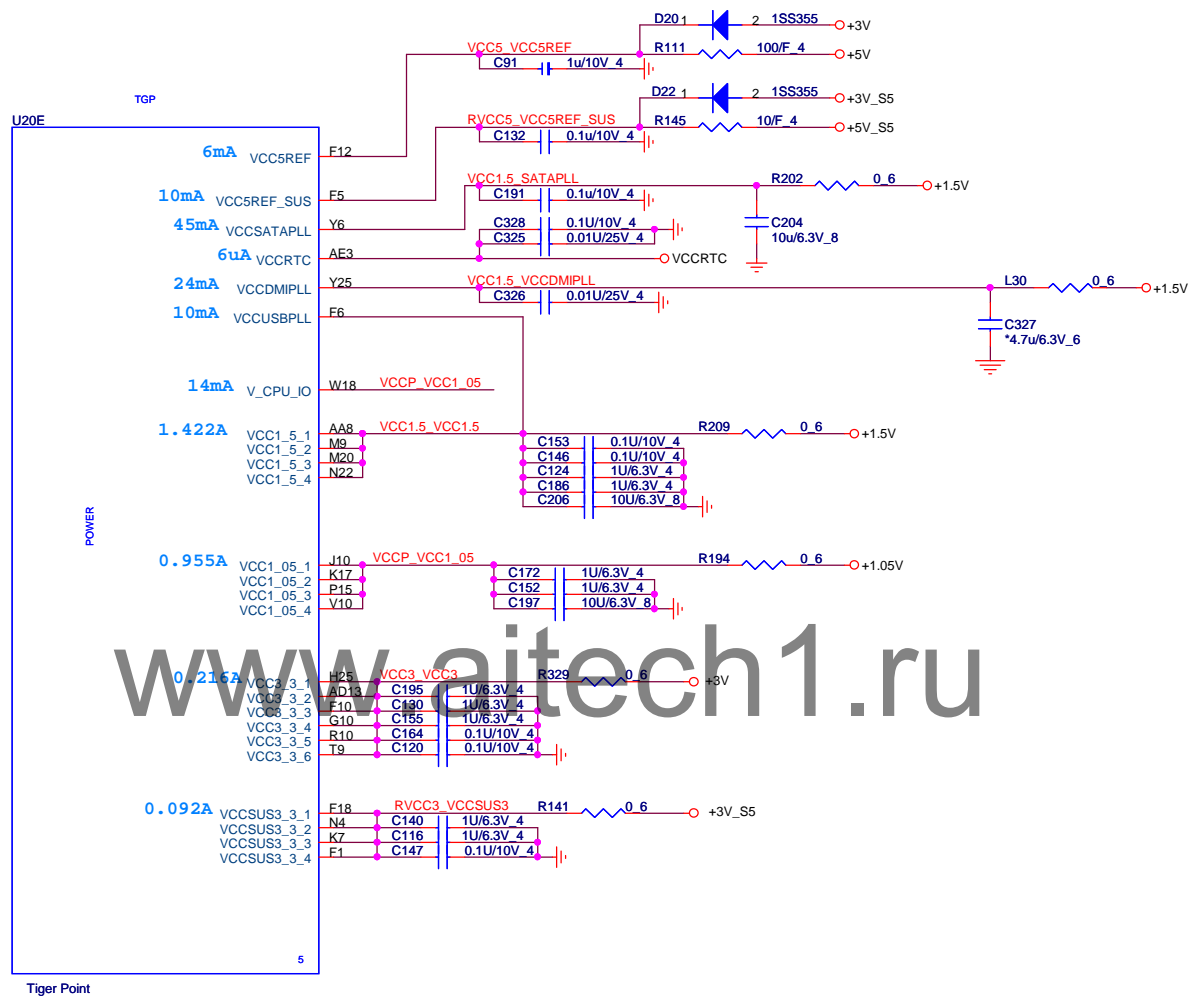
INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

Quanta Computer Inc.
PROJECT : ZGA

Size: Document Number: TigerPoint GPIO
Date: Wednesday, July 07, 2010 Sheet 12 of 38

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH



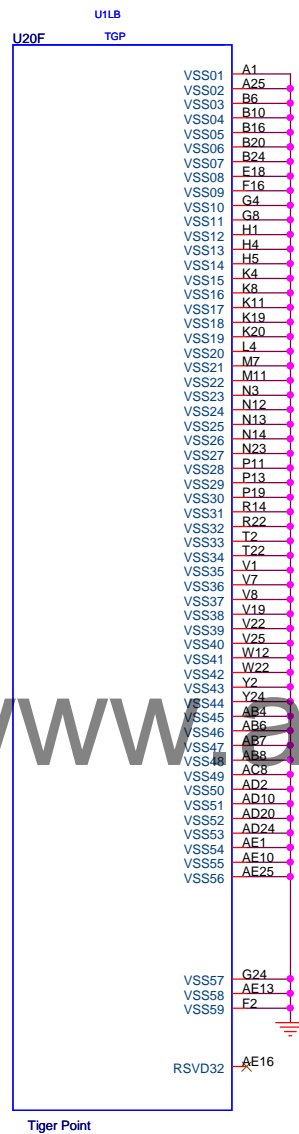
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




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PROJECT : ZGA

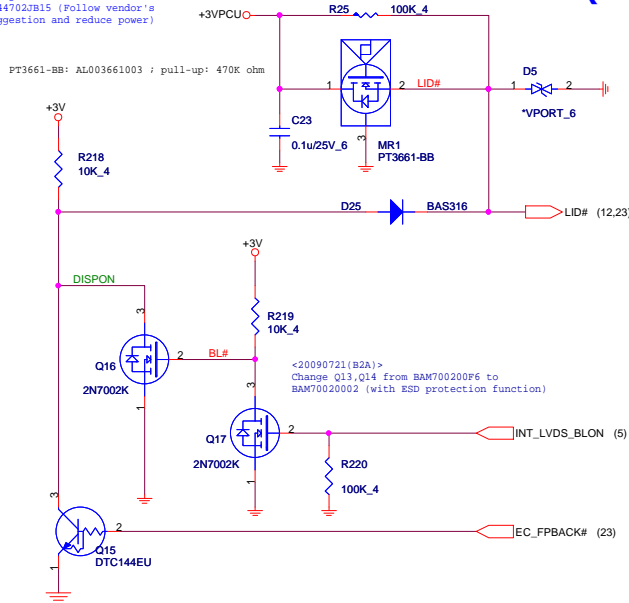
Size	Document Number	Rev
		1B
TigerPoint Power		
Date:	Wednesday, July 07, 2010	Sheet 13 of 38



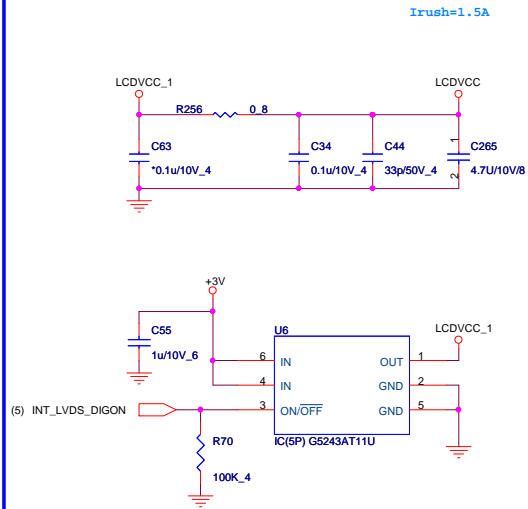
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 Quanta Computer Inc. PROJECT : ZGA		Rev
		1B
Size	Document Number	
TigerPoint GND		
Date:	Wednesday, July 07, 2010	Sheet 14 of 38

HALL SENSOR(HSR)

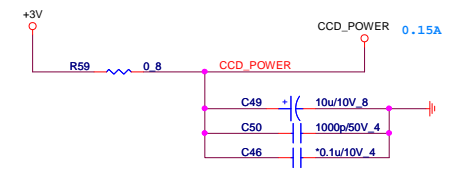


LED Panel POWER SWITCH(LDS)

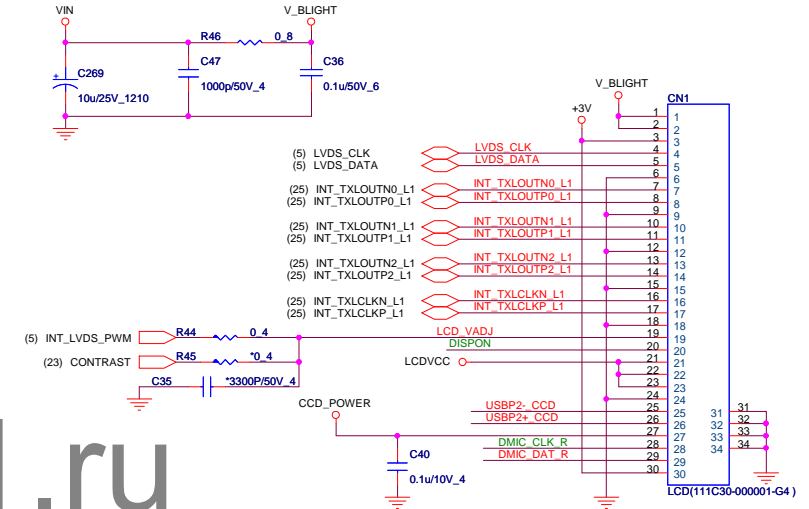


CAMERA POWER(CCD)

14



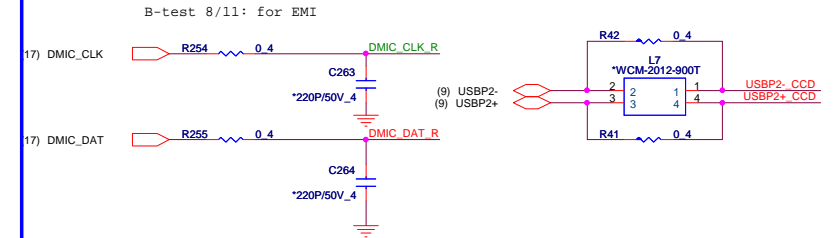
LED Panel(LDS)



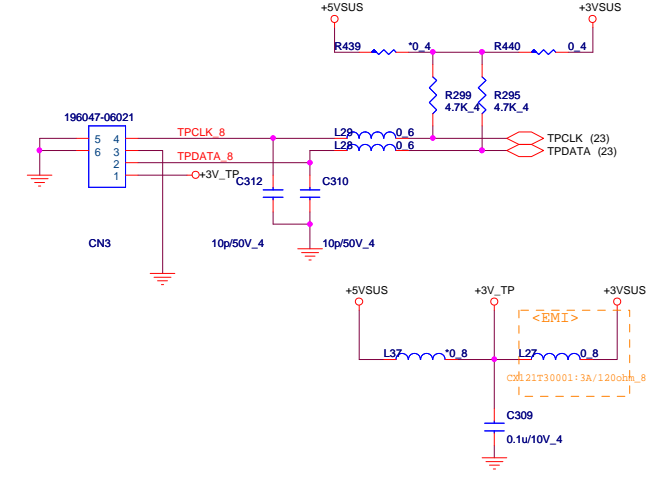
CRT(CRT)

3/11 : cancel CRT function

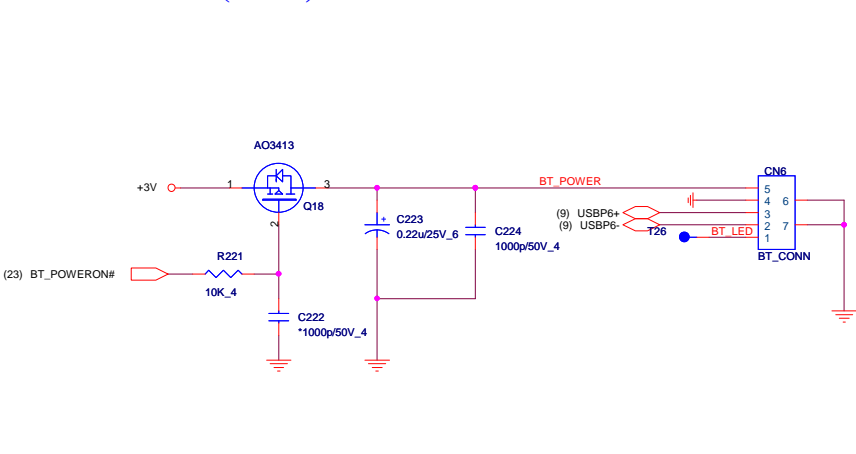
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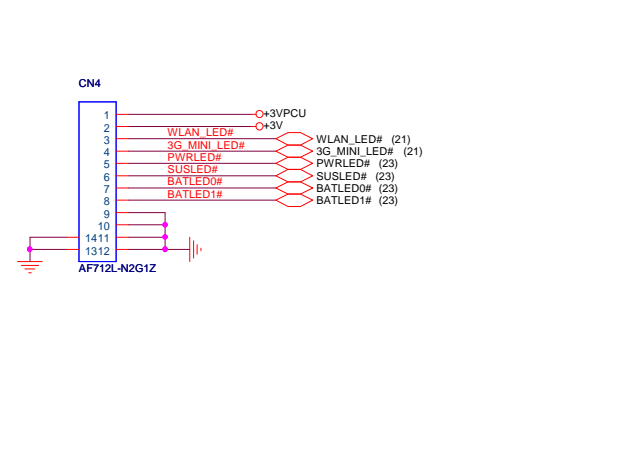
TOUCH PAD(TPD)



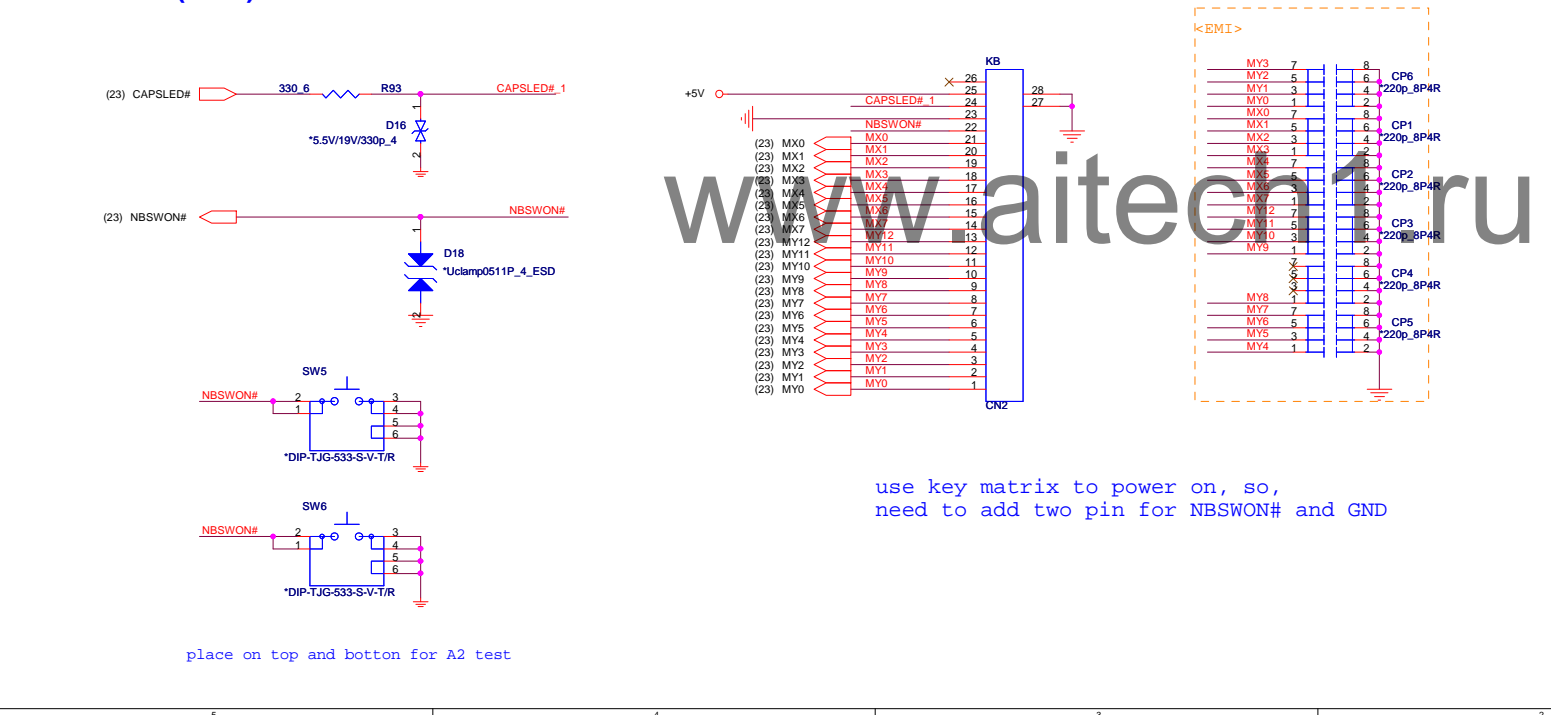
BLUETOOTH(BTM)



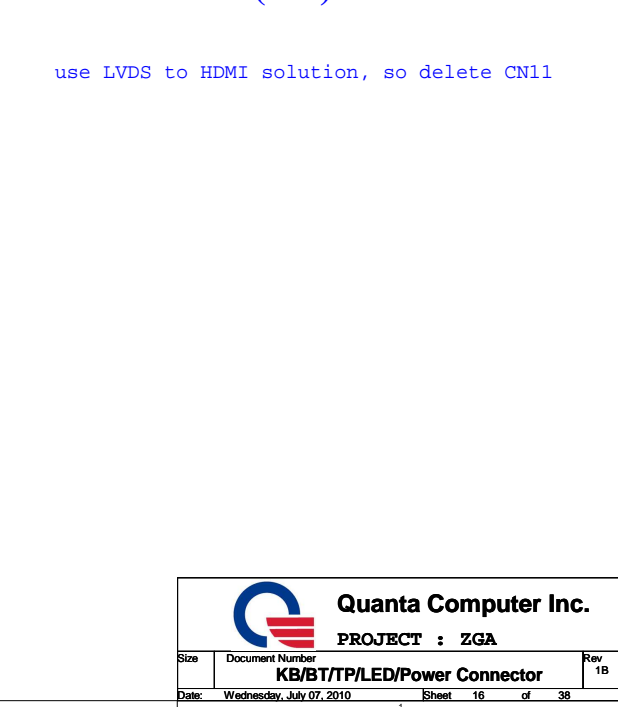
Connector (UIF)



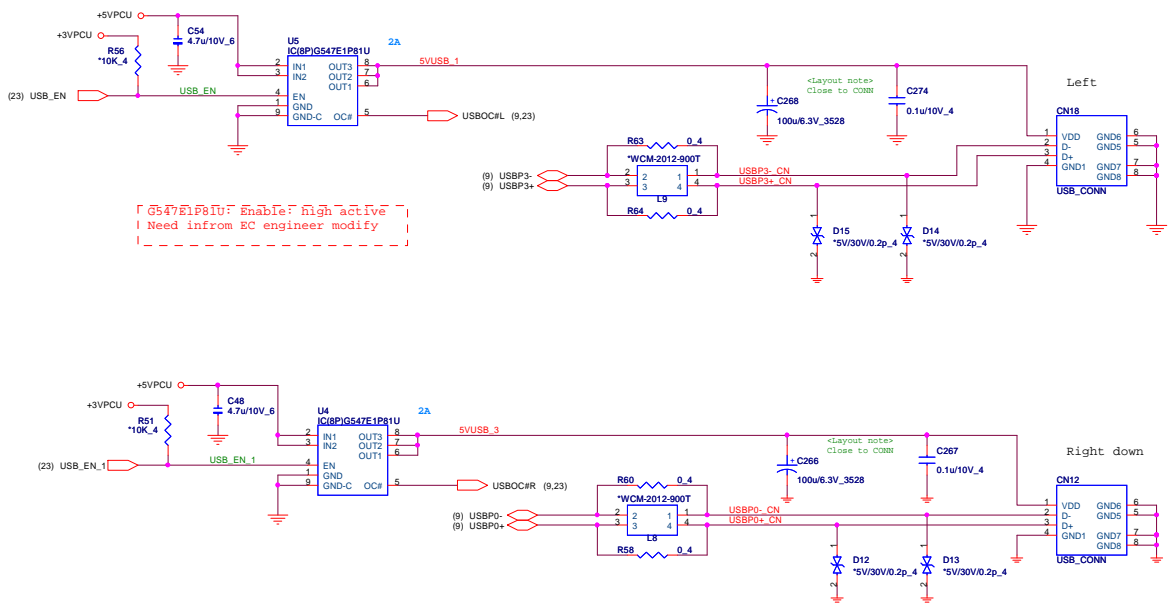
KEYBOARD(KBC)



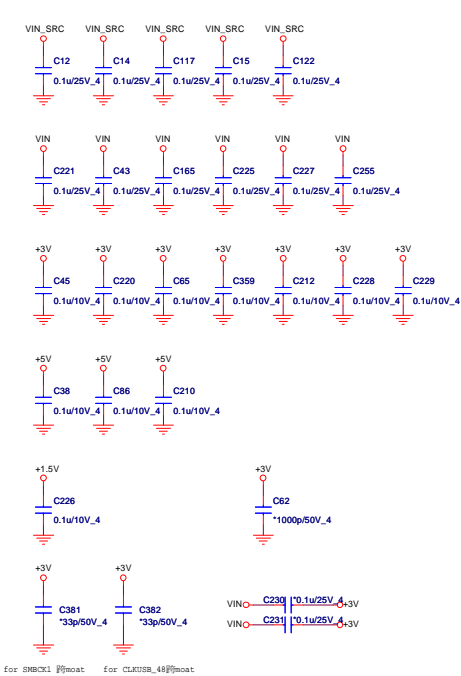
RGB to HDMI(DB)



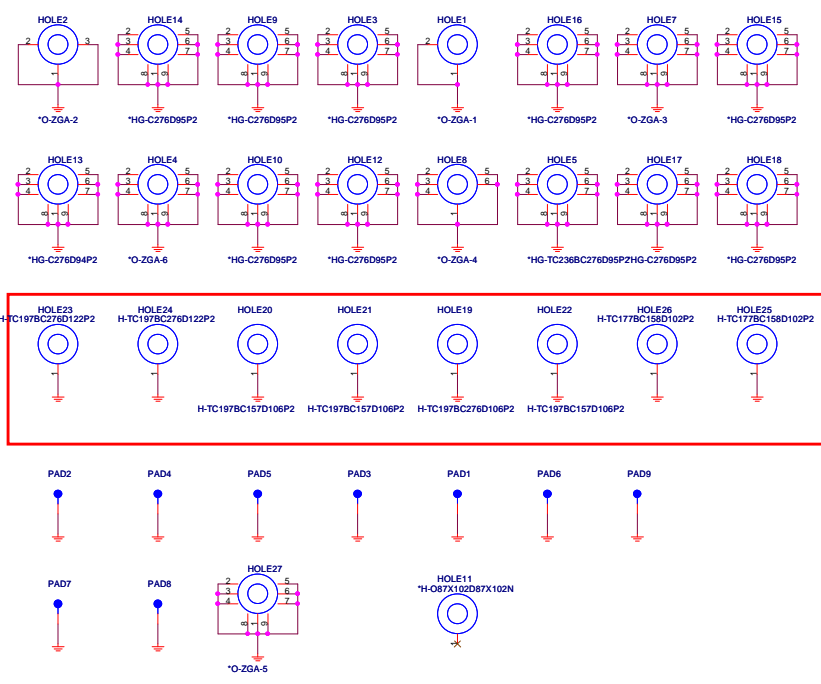
USB(USB)



EMI



Hole



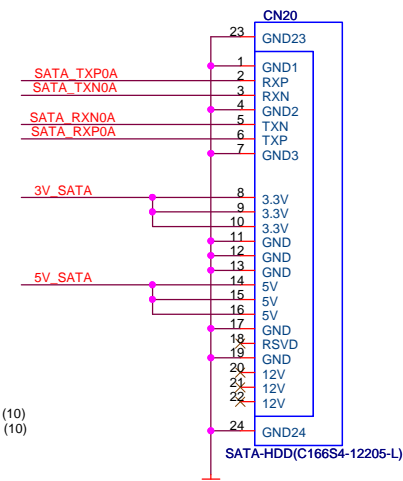
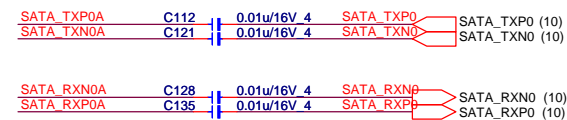
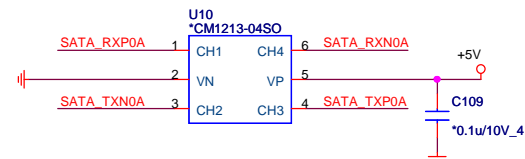
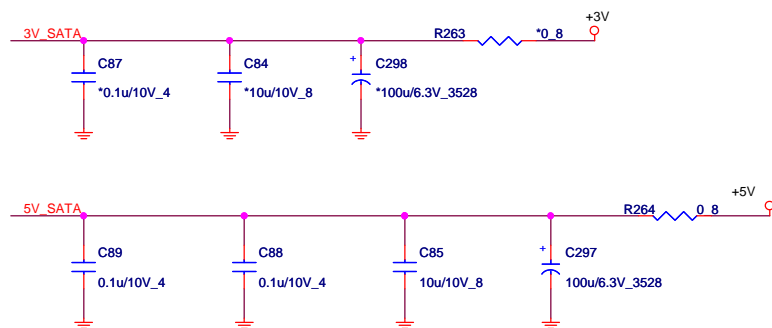
www.aitech1.ru

Giga-LAN AR8151(LAN)

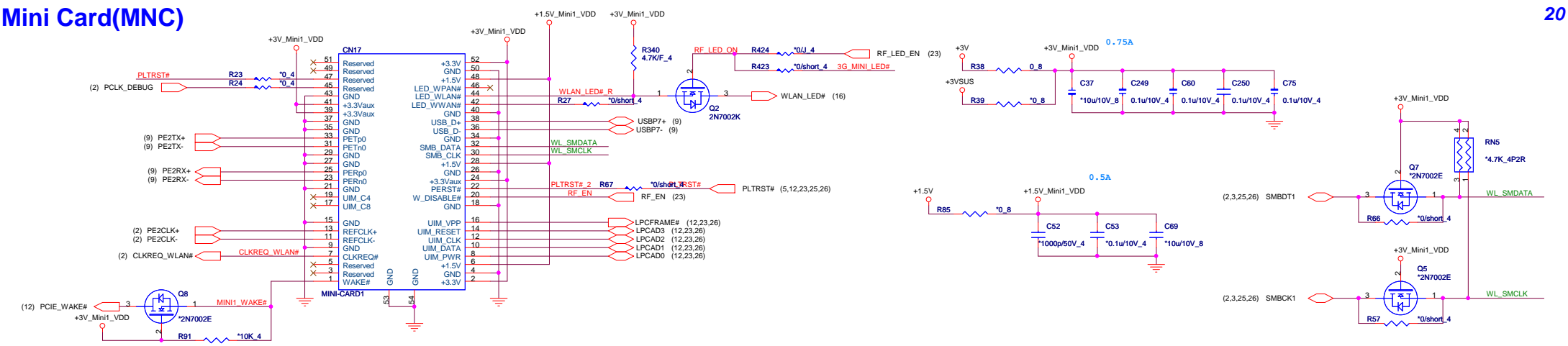
TRANSFORMER(LAN)

RJ45(LAN)

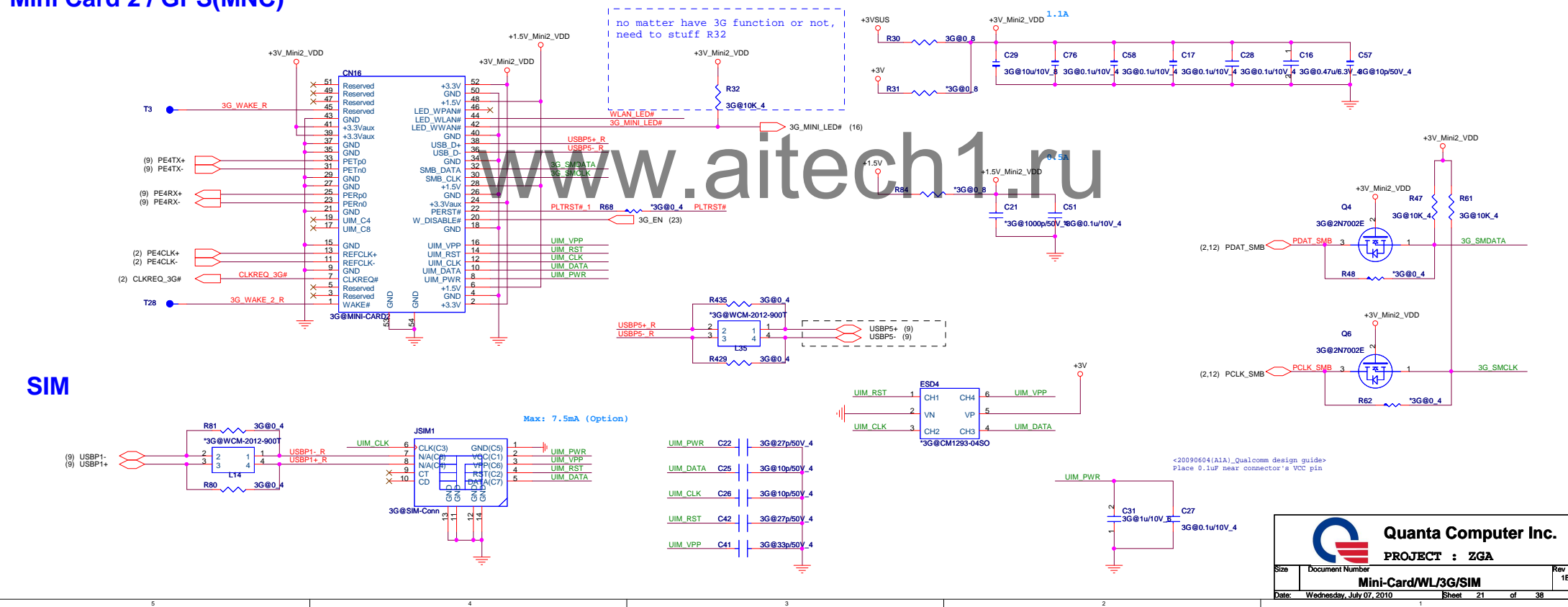
www.aitech1.ru



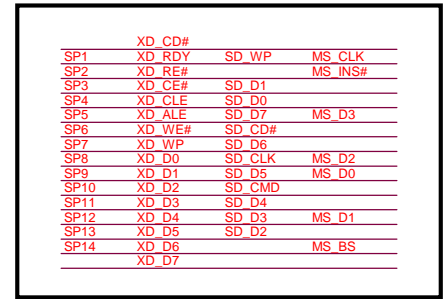
www.aitech1.ru



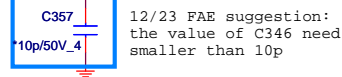
Mini Card 2 / GPS(MNC)



RTS5138



Share Pin

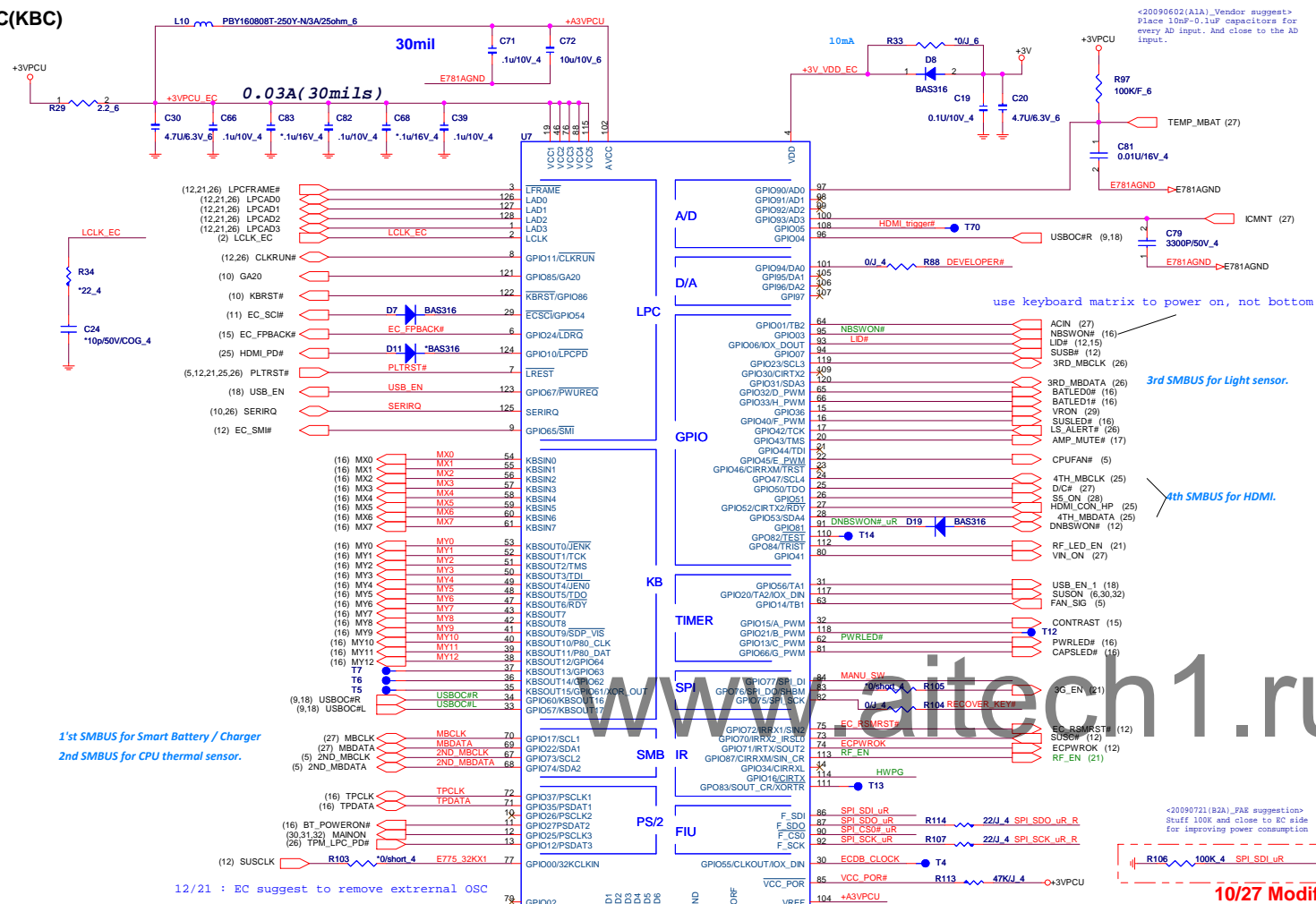


```
01/29 change connector pin define
Main:DFHS44FR012
```

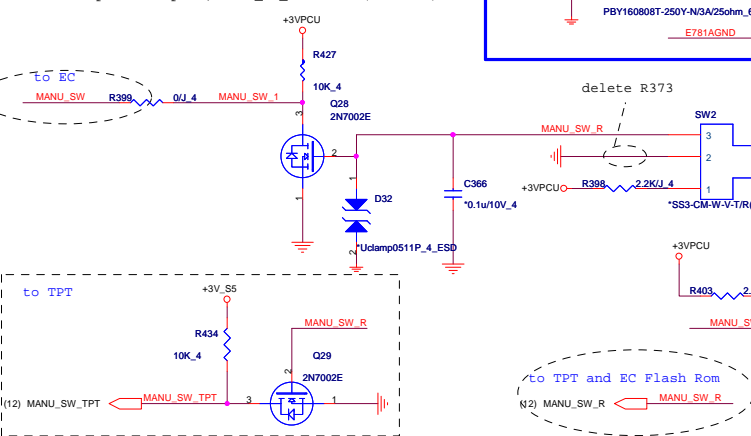
03/11 change connector footprint for Dip type.

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EC(KBC)

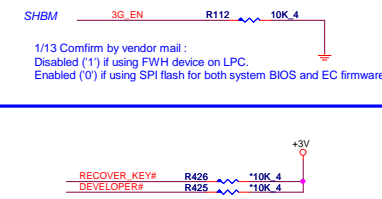


```
SW2 : connect pin2 and pin3, MANU_SW_R is high.  
      connect pin1 and pin3, MANU_SW_R is low.(default)
```

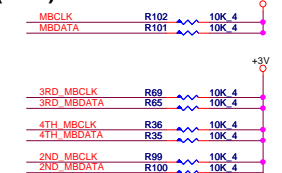


I/O ADDRESS SETTING(KBC)

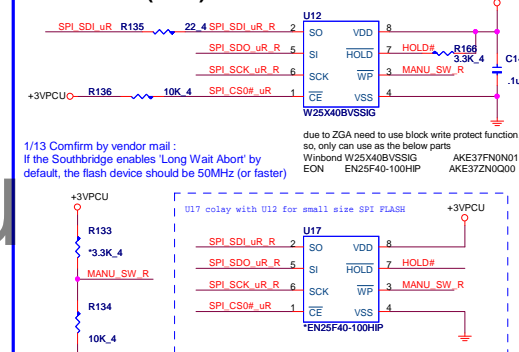
SHBM=0: Enable shared memory with host BIOS



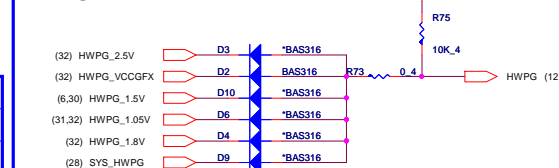
SM BUS PU(KBC)



SPI FLASH(KBC)



HWPG




SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor
SM Bus 3	Light sensor

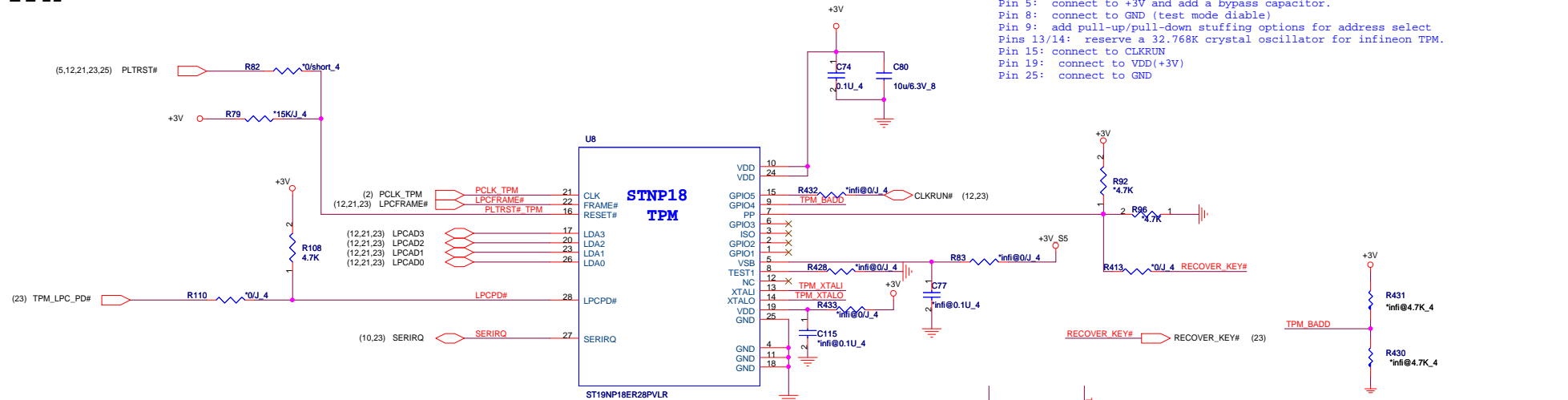
INTERNAL KEYBOARD STRIP SET(KBC)



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		Quanta Computer Inc.	
		PROJECT : ZGA	
Size	Document Number	HDMI(1/2)	Rev 1A
Date: Wednesday, July 07, 2010		Sheet	24 of 38

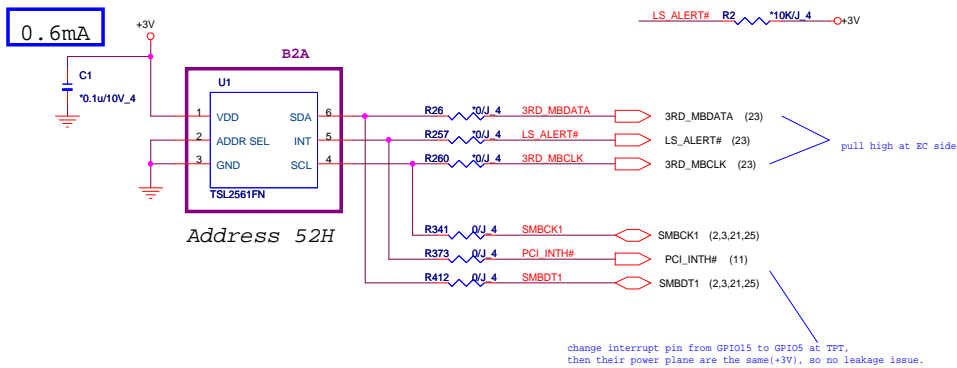
TPM



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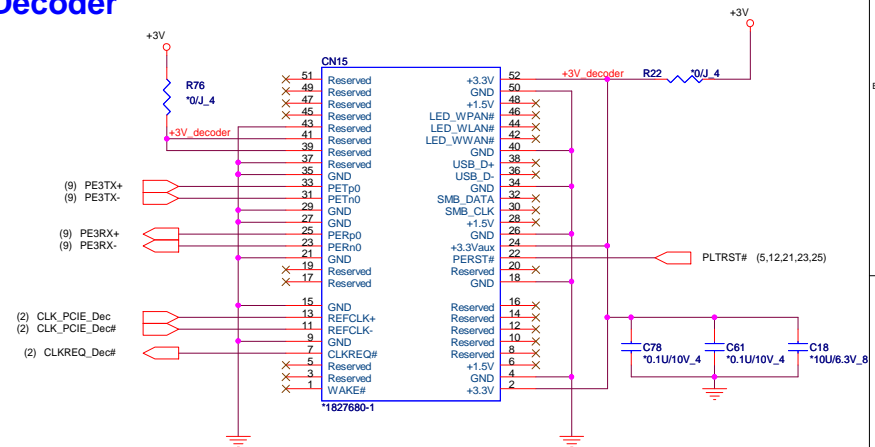
Light Sensor(LSR)

connector to EC, just stuff R2,R26,R257,R260
 connector to TPT, just stuff R341,R373,R412

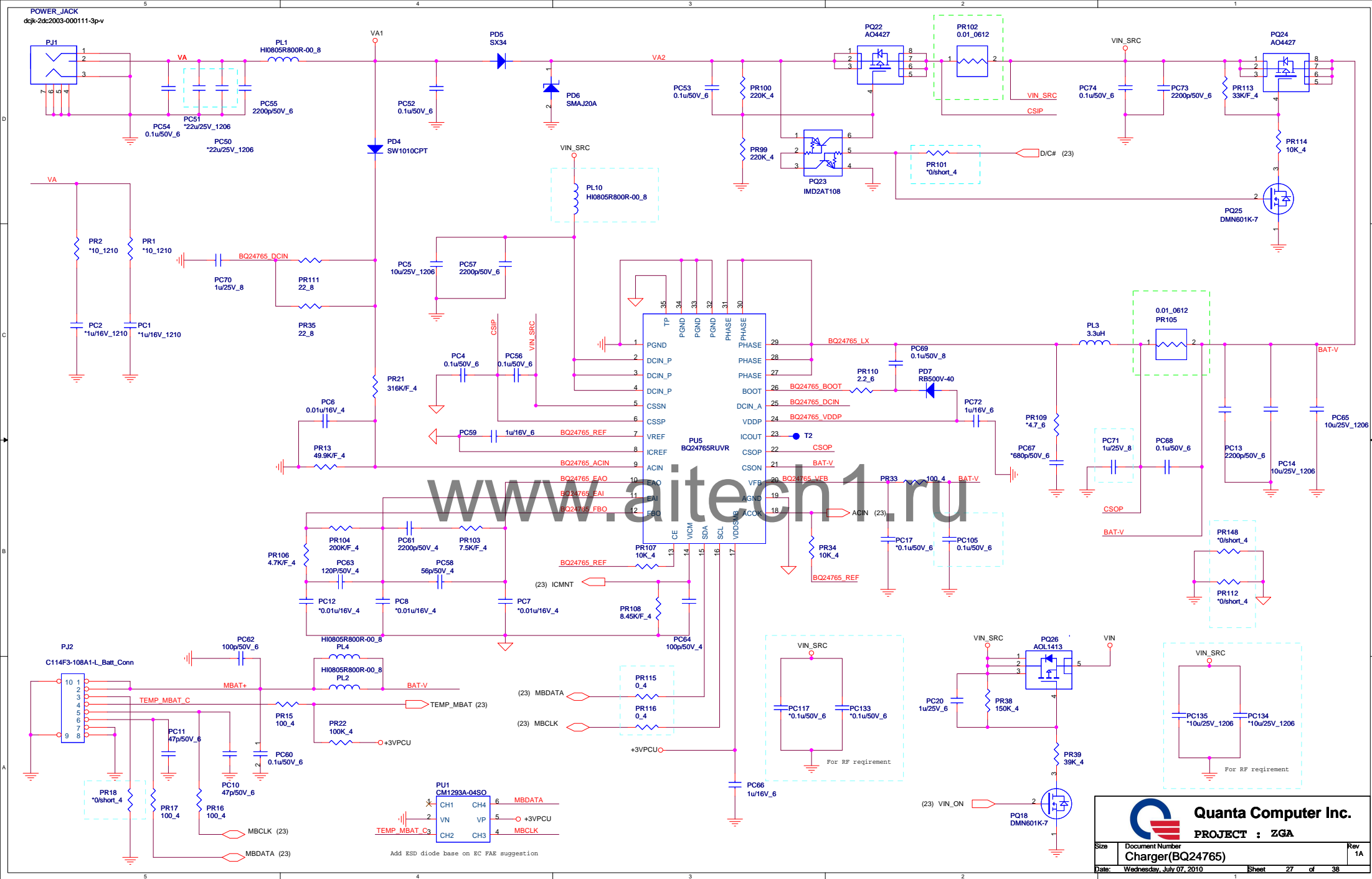


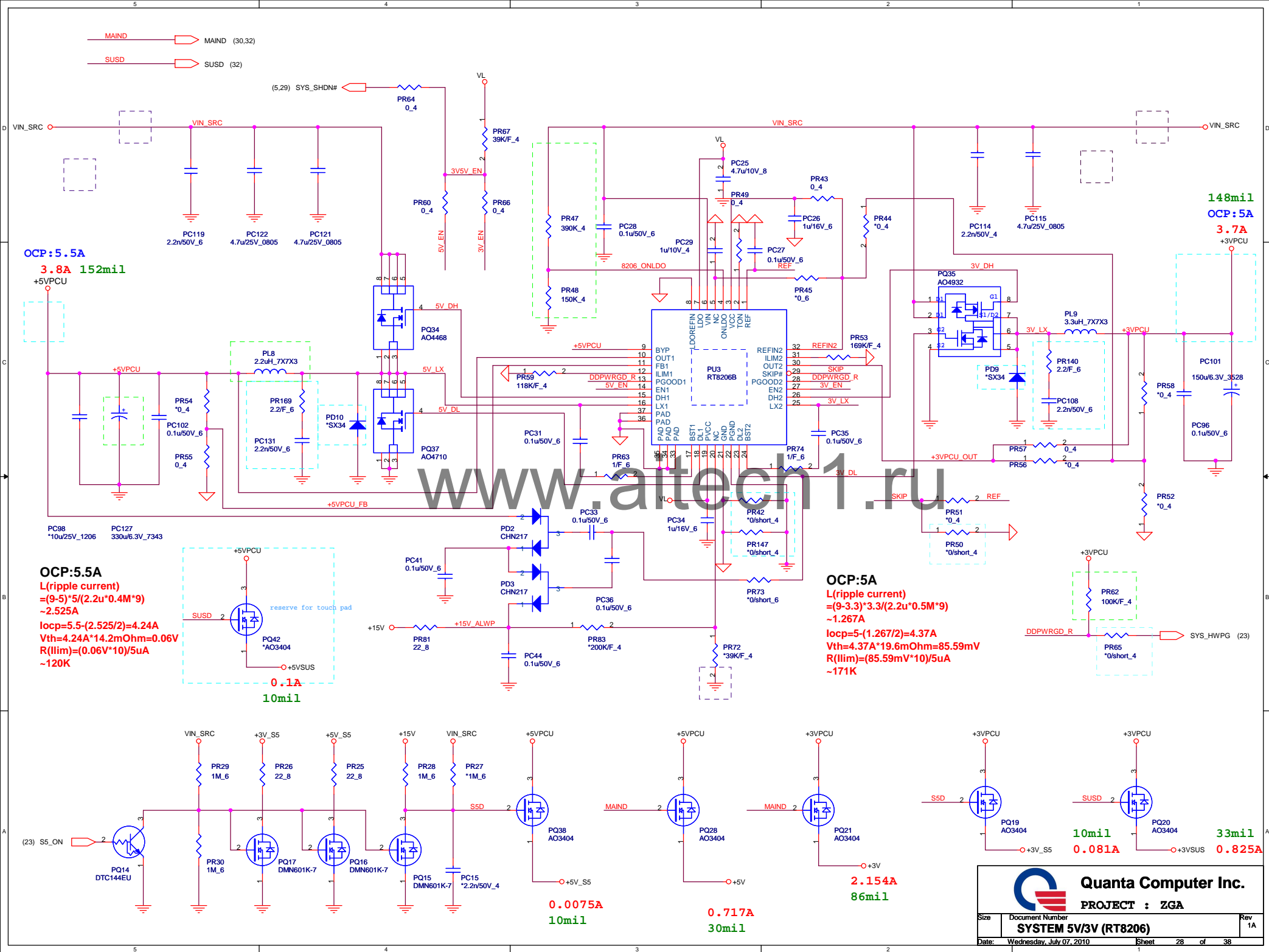
Video Decoder

dont need to stuff first, use innr document to add it.

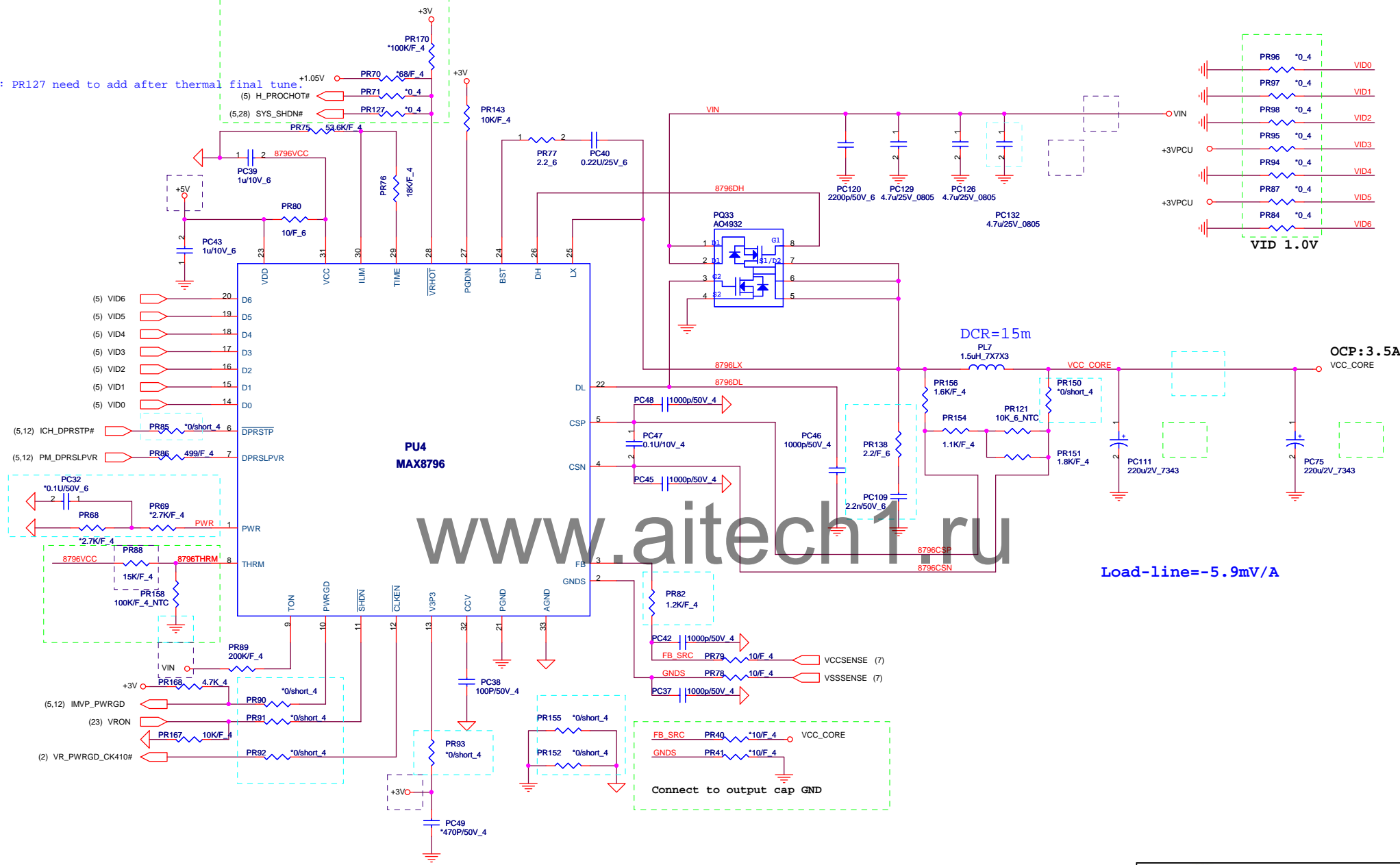


	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F



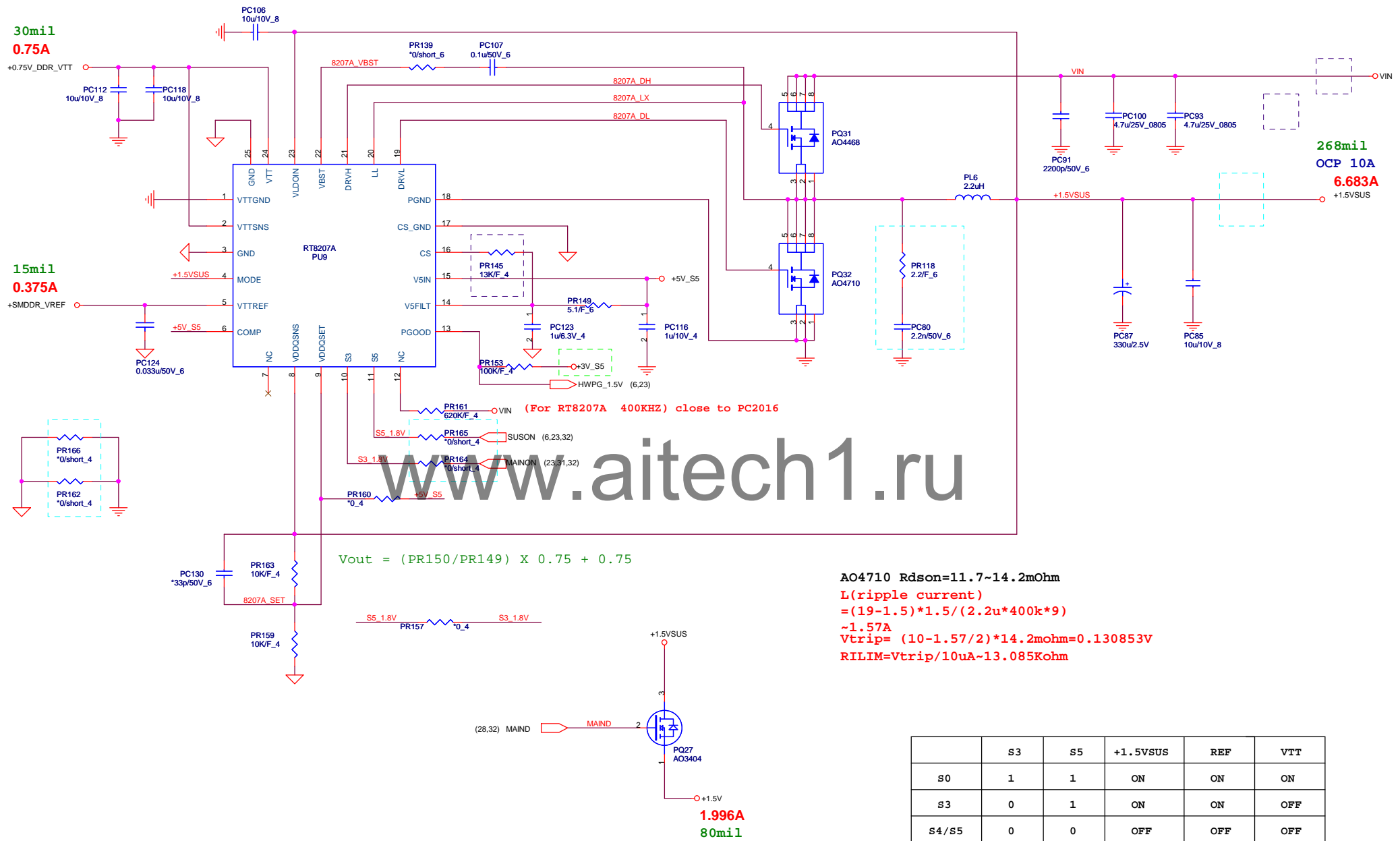


6/24 : PR127 need to add after thermal final tune



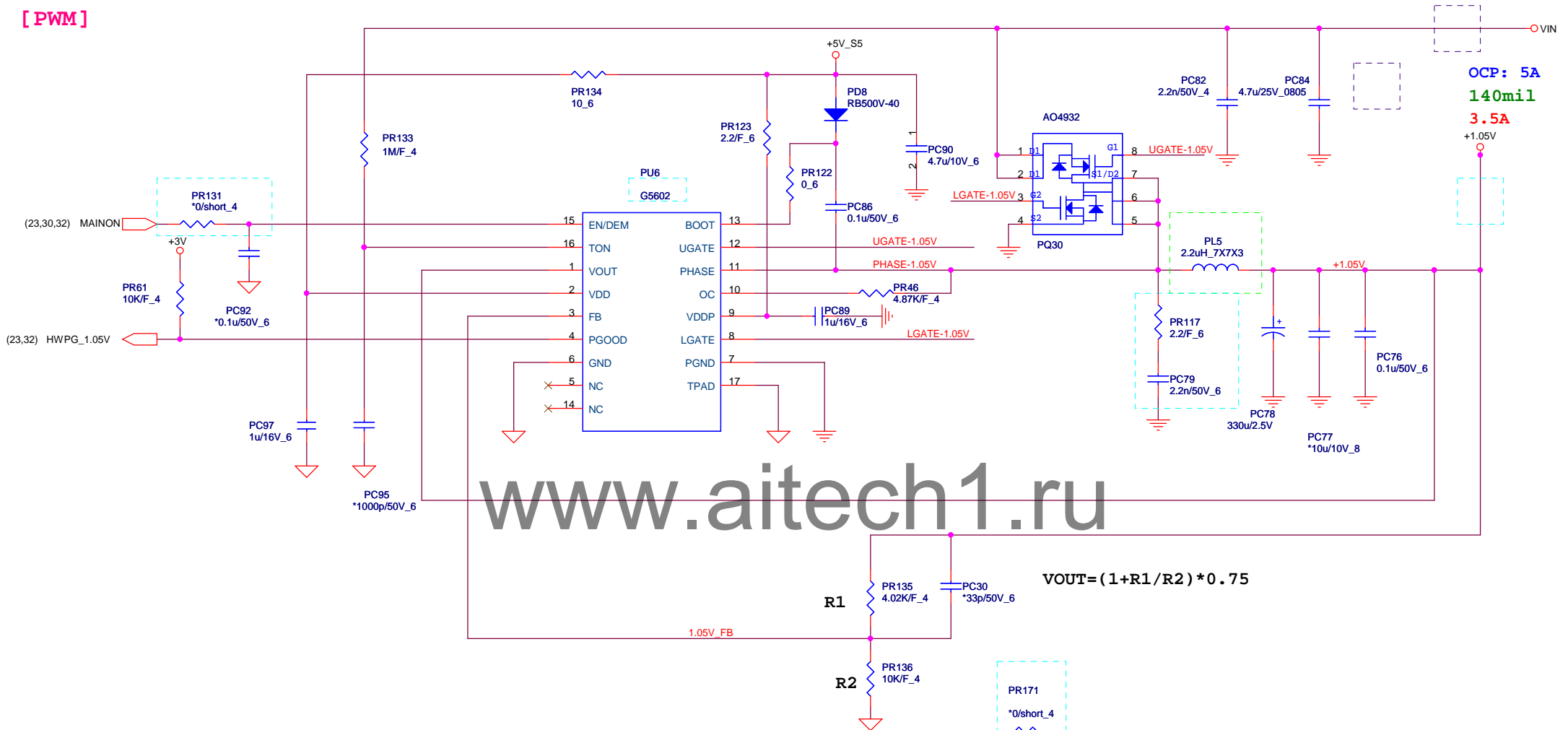
Load-line=-5.9mV/A

[PWM]



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

[PWM]



$$TON = 3.85p \cdot R_{TON} \cdot V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO4932 $R_{dson} = 15.8 \sim 19.6m\Omega$

$$L(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (2.2u \cdot 272k \cdot 19) \sim 1.658A$$

$$R_{th} = 19.6m \cdot (5 - 0.829) / 20uA$$

$$R_{ILIM} = 4.087K\Omega$$

$$V_{OUT} = (1 + R1/R2) \cdot 0.75$$

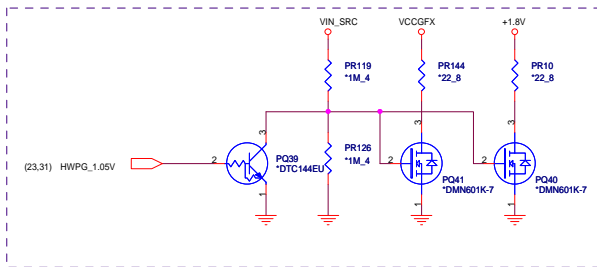
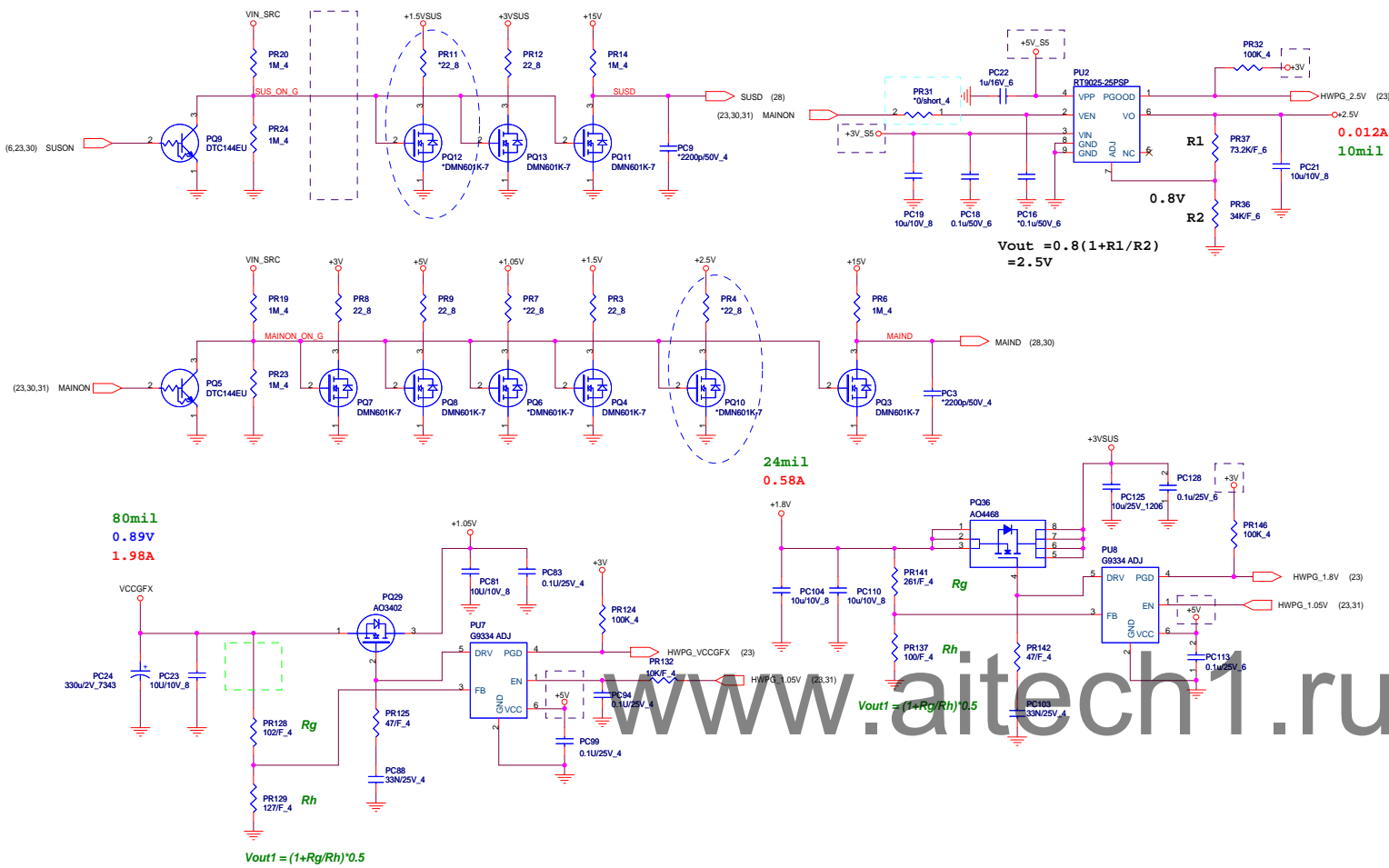


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PROJECT : ZGA

Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1A

Date: Wednesday, July 07, 2010 Sheet 31 of 38



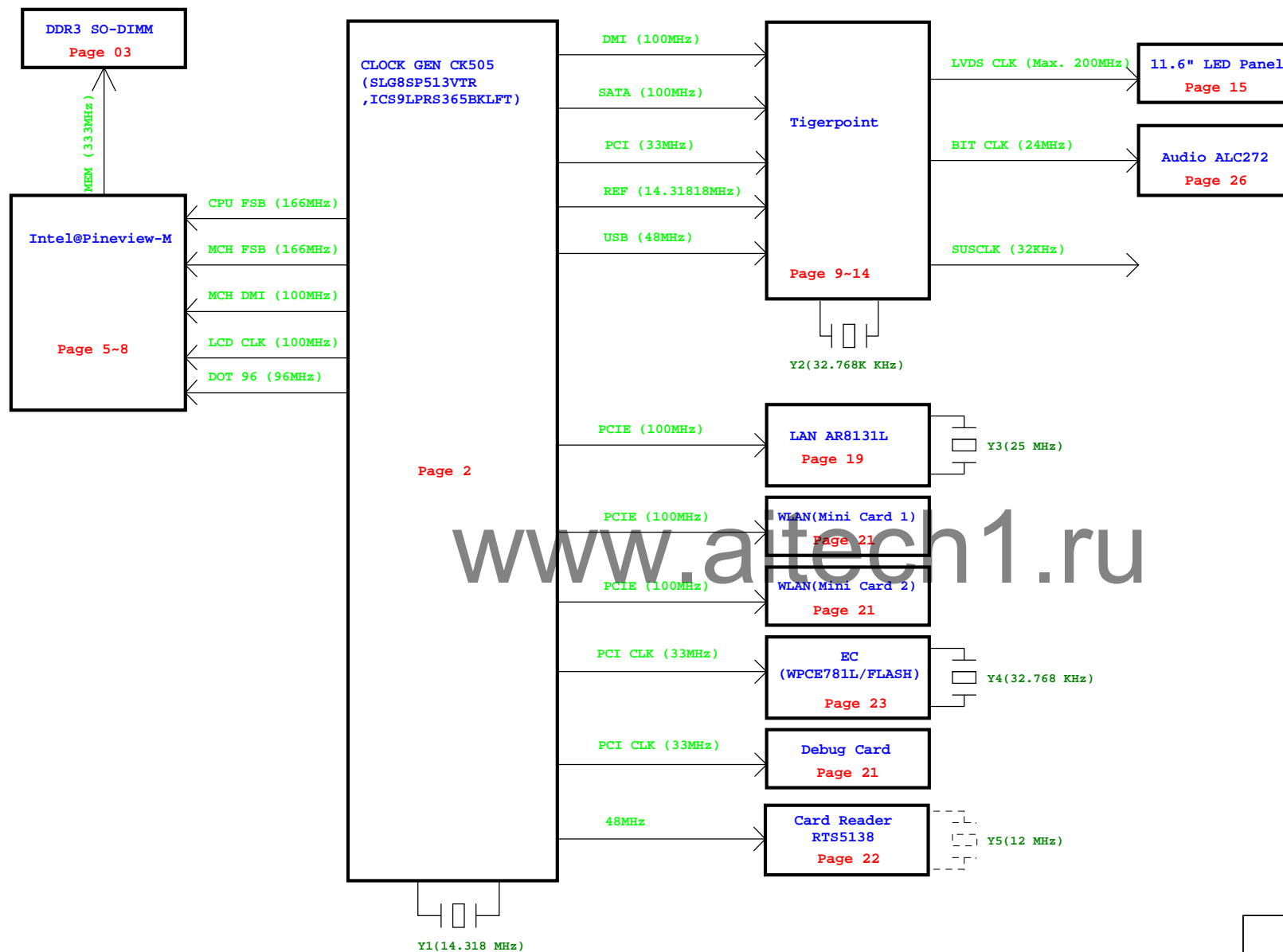
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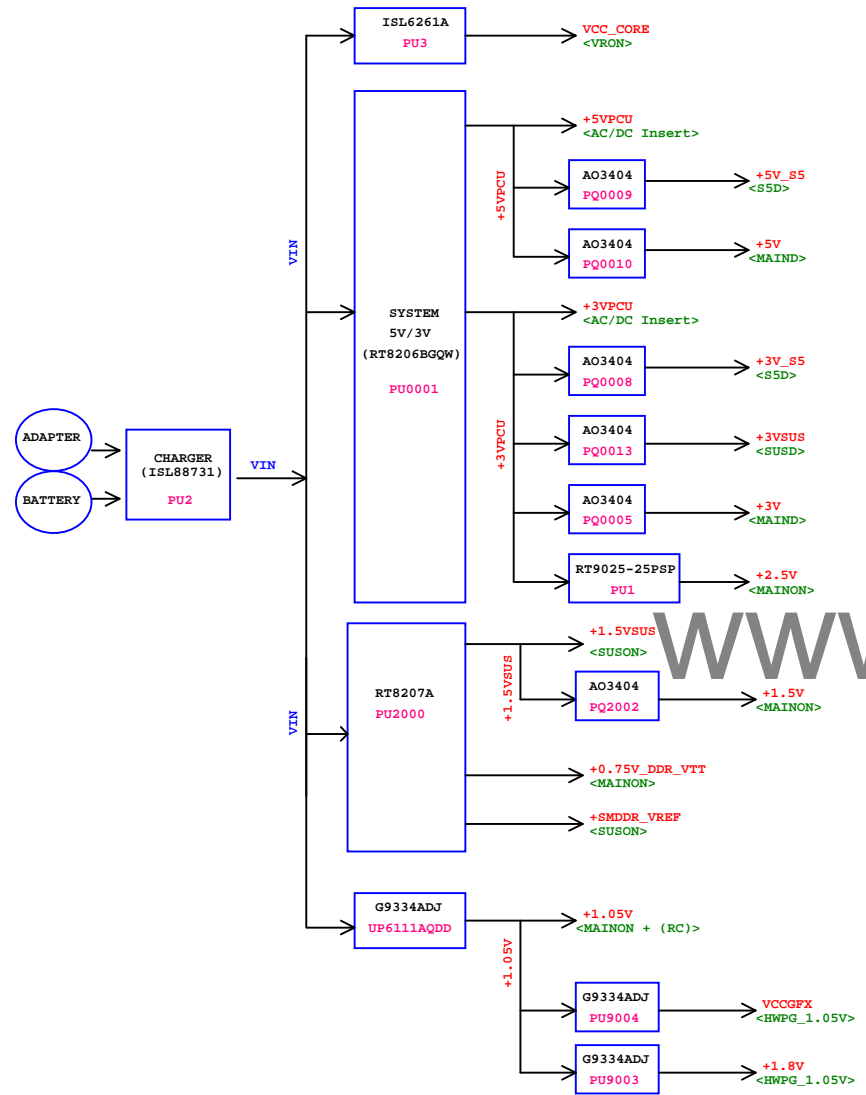


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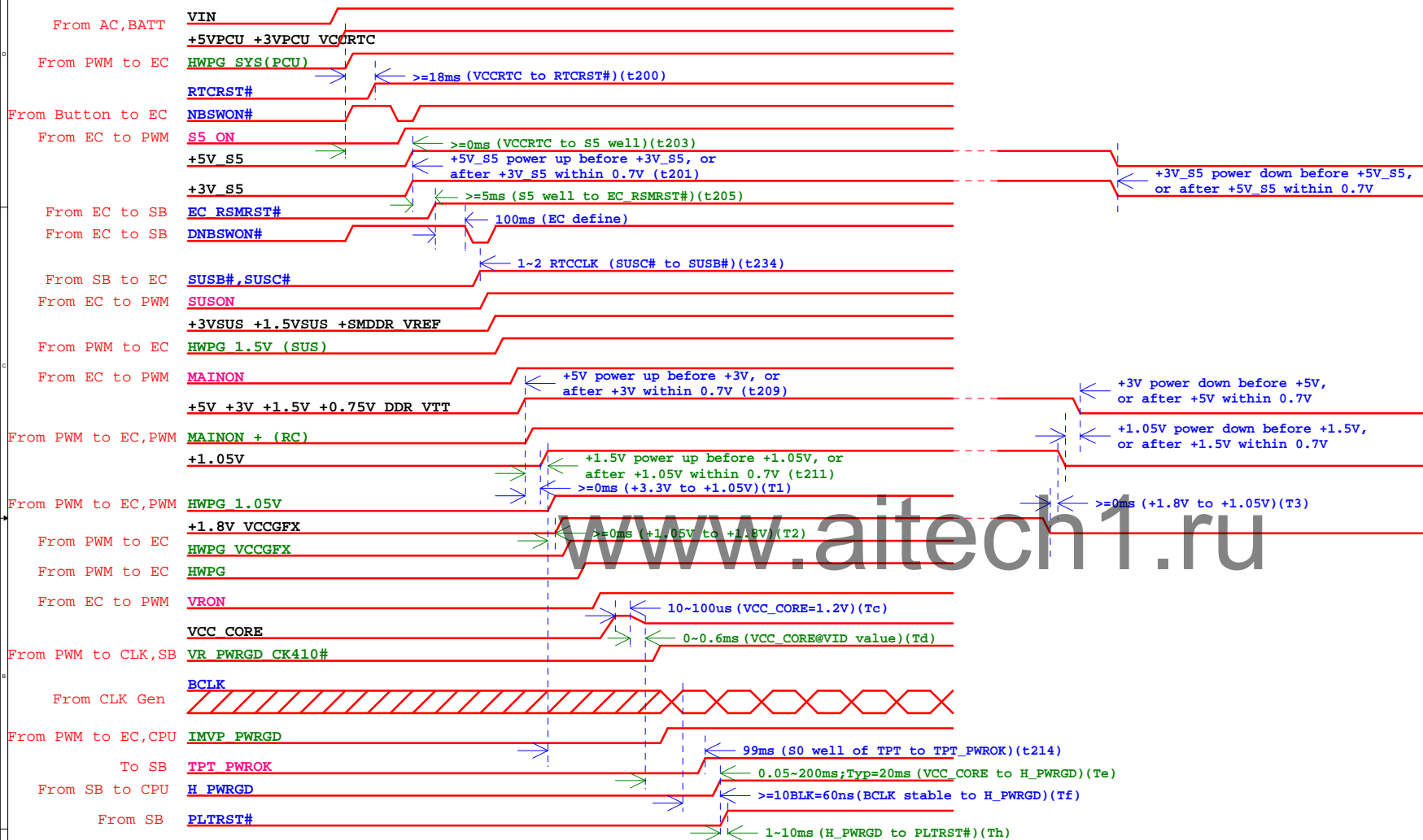
PROJECT : ZGA

Size	Document Number	Rev
	Blank	1A
Date:	Wednesday, July 07, 2010	Sheet 33 of 38





POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connector
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.5V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	Light Sensor
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT (Level shift)	X	X	X



[illegible]